# AN AUTOMATIC TESTER FOR DIGITAL INTEGRATED CIRCUITS

A Thesis Submitted
In Partial Fulfilment of the Requirements
for the Degree of
MASTER OF TECHNOLOGY

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to the
DEPARTMENT OF ELECTRICAL ENGINEERING
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SEPTEMBER, 1973

## CERTIFICATE

Certified that this work on "AN AUTOMATIC TESTER FOR DIGITAL INTEGRATED CIRCUITS" by Mr. P.K.Sridharan has been carried out under my supervision and that this has not been submitted elsewhere for a degree.

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## ACKNOWLEDGEMENTS

I express my deep sense of gratitude to Dr.R.N.Biswas for his unfailing guidance and keen interest he evinced during the course of this work. I wish to thank all my friends who have contributed in different ways to the completion of this work. I also thank Shri Pandey for having done an excellent job of typing.

P.K.SRIDHARAN

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## ABSTRACT

An attempt has been made to develop an automatic tester for Digital Integrated Circuits in this project. The two aspects of static testing of digital IC's viz- Functional Testing and Parametric Testing have been studied in detail, and the necessity as well as the advantage of hardware programming has been established. The implementation of hardware programming has been carried out using plug-in printed cards.

A Functional Tester incorporating the above concept has been built with indigenously available integrated circuits. A pattern generator, reference generators and comparators form the basic blocks of this tester. The reference outputs for most of the gates and flip-flops belonging to the 7400 series of TTL family have been generated internally, while provision has been made to test any digital circuit which has a maximum of 8 inputs and upto 4 outputs, by externally feeding the reference outputs.

The principle of automatic parametric testing and the system design of a Parametric Test Unit have also been given. By choosing a repetitive ramp voltage as input, with a three fold sequencing of tests and with forced current loading at the output, the possibility of testing any multiple, multi input NAND/NOR gate chip under all loading conditions has been brought out.

# CHAPTER-I

# INTRODUCTION

## 1.1 MOTIVATION FOR THE PROJECT

An Integrated Circuit (usually abreviated as'IC') is a product fabricated by sophisticated mechanical and chemical processes and is intended to perform a complex electrical function. As a product, it is subject to statistical variations as well as to changes brought about by environmental conditions, mainly temperature. As a consequence, in most places where IC's are either manufactured or used in large quantities, there is a growing need for a quick testing of IC's. For the manufacturer this becomes the final stage of his quality control programme, where the packaged device has to be given a final check before being sent out. On the other hand, the user needs such a test set up in order to ensure that the devices being put in his system will perform the functions required of them. The importance of such prior check will be evident from the following considerations.

Assume that on the average 2% of the incoming IC's are bad (which is a fairly common figure) i.e. one out of fifty IC's will be bad. Then if, on the average ten IC's

are to be mounted in each circuit card, one out of every five cards may be expected to malfunction. The cost of troubleshooting and replacing the bad IC's will easily be far in excess of what the IC user would have to spend to test incoming IC's.

Clearly, it would be preferable if such testers can be handled by relatively unskilled operators. A GO/NO-GO type of tester in which indicating lights are turned on upon failure of the test/tests is ideally suited for this purpose. Conventional manual testing involves the use of curve displays and are as such laborious and time consuming. A practical IC tester to meet the above requirements will therefore have to incorporate the concept of preprogrammed automatic testing.

## 1.2 AUTOMATIC TESTING[1]

Any test system should meet the following requirements.

1. Correct biases and limits for the device under test must be established.
2. Measurements made must be accurate.
3. Some classification criteria must be applied.
4. Data about test results must be recorded.

In an automatic test system all these requirements are met in an appropriate sequence automatically, i.e. without manual intervention at any stage. All these are

to be done with due regard to the safety of the device under test and to the operator. The essential features of an automatic IC test system are given below.

1.2.1 Speed

Speed is the most obvious factor, particularly in places where IC's are made or used in large quantities. Here a distinction has to be made between test speed and handling speed. Even the slowest test system is so fast that the entire series of tests may be over in a few milliseconds. But high test speed in itself does not provide an overall high speed test system. This is because the time required to remove a device from the test station and insert another is usually many times greater than the actual testing time. To overcome this limitation many high volume testers incorporate automatic handling facilities and provide for some degree of multiplexing or the simultaneous use of two or more test stations with a single test system.

1.2.2 Programming

Since IC's generally require a long sequence of complex tests, preprogramming of the test procedure is necessary in any automatic test system. This programming may be done either by means of hardware or through software using any of the input media, e.g. punched cards, paper tape, magnetic tape etc. The programming is typically done

by the test system manufacturer, although provision is made sometimes for the skilled user to program his own test conditions.

### 1.2.3 Data logging

The results of IC testing can be displayed either on a GO/NO-GO basis or as actual parametric measurement. For GO/NO-GO test, the test result is compared with high/low test limits to determine its acceptability and indicating lights are turned on upon failure of test/tests. Collection of data about test results may be very useful for the manufacturer, and sometimes to the user also, to perform some evalution studies about the device. Such data can be displayed either as histograms on a type writer or parameter distribution curves on a graphic terminal and the manufacturer can use this information to monitor his profuction process and for his quality control programme.

## 1.3 SCOPE OF THE PROJECT

In this project an attempt is made to develop a GO/NO-GO type of tester for Digital IC's which will be particularly useful for small scale industries and research institutions. Such a GO/NO-GO type of tester is well suited for Digital IC's since the complete truth table as to whether the IC is good or not can be easily formed for the device.

Since gates and flip-flops form the basic building blocks of any digital system, only the testing of these devices has been considered. Moreover we have restricted the test set up only to the TTL family which is the most popular among all Digital IC logic families and is also the most versatile in applications. It is, atleast in the present state of art in India, the only indigenously available family. Of course there is no reason why the tester can not be used for DTL family as well.

The important characteristics of gates and flip-flops are discussed in Chapter II. Chapter III is devoted to a brief discussion of the various tests that are normally done on digital IC's,their relative importance and the techniques used for embedding the D.U.T in an automatic tester . The complete design of the functional testing set up is presented in Chapter IV. The measurement schemes for some of the parameters of the gate, with emphasis on suitability for automatic testing, are discussed in Chapter V. Chapter VI deals with the design of the parametric test instrument. In Chapter VII, a critical evaluation of what has been achieved in this project has been attempted, and future possibilities of modification, expected to bring about improvements have been suggested.

# CHAPTER-II

## CHARACTERISATION OF DIGITAL IC'S

### 2.1 GENERAL FEATURES

A device that switches between two exclusive states usually represented by logic 1 or 0 is called a digital device. Normally operation of a digital device can be represented by what is called the truth table which gives the relationships between inputs and outputs. With the introduction of integrated logic elements there is no need, at least for certain class of users, to go into the circuit details of these elements as long as the terminal properties are clearly defined.

Neverthless, in practice it is often useful for designers to be familiar with the electrical properties of the digital IC and also some of the problems and limitations which are encountered in the use of such circuits.

A logic gate is the building block of all digital circuits. The performance of both NOR and NAND gates can be characterised in terms of the corresponding NOT or Inverter circuit since the response would always be the same as long as the NOT circuit has an equivalent input.

The criteria used for evaluating the performance of a particular digital logic family are therefore based on the characteristics of the basic inverter of that family. Hence before going for the actual testing and measurement procedures necessary for any digital logic family, it is essential at this stage to consider some of the basic electrical properties of the inverter of the family.

Since an inverter is a two port device, its static behavior can be completely characterised by its (i) input characteristics (ii) output characteristics and (iii) the transfer characteristics.

## 2.2 (INVERTER) INPUT CHARACTERISTICS.

The input characteristics can be represented by the plot of input current versus input voltage. Since an inverter is normally expected to be in either of the two extreme states (logical 0 and logical 1), one is usually concerned mainly with input currents in these extreme states. These are denoted by $I_{iL}$ and $I_{iH}$ corresponding to low and high levels of the input voltage respectively. The direction and magnitude of these currents may be different in different logic families. The motivation for measurements of $I_{iL}$ and $I_{iH}$ arises because these measurements give an insight into the voltage limitation and power handling capabilities of the input port.

## 2.3 (INVERTER) OUTPUT CHARACTERISTICS

All uses of gate circuits involve interconnections of similar units and the rules which must be used when interconnecting the elements of a logic family are called "Loading Rules" for that family. They include the definition of the output capabilities of the elements of the family together with the load presented by each type of input. Such description can be simplified by the introduction of the concept of unit load. Normally a gate input is said to require one load, and the number of simlar gates that can be driven by its output is called the FAN OUT of the gate. When the fan out of the gate and the input currents $I_{iL}$ and $I_{iH}$ are specified, there is no need to specify the output port v-i characteristics since the output of the gate is normally connected to inputs of similar gates. The most important output characteristics are the output voltage levels of the gate under various loading conditions.

## 2.4 (INVERTER) TRANSFER CHARACTERISTICS

The transfer characteristic of a gate circuit contains a wealth of information about the properties of the gate and is usually used as the criterion for evaluating the performance of the gate. Generally the shape of the characteristic is as shown in Fig. 2.1.

$V_{IL}$ is the guaranteed maximum input voltage level upto which the output voltage is above the minimum permissible level for logical 1

$V_{IH}$ is the guaranteed minimum input voltage level upto which the output voltage is below the maximum permissible level for logical 0.

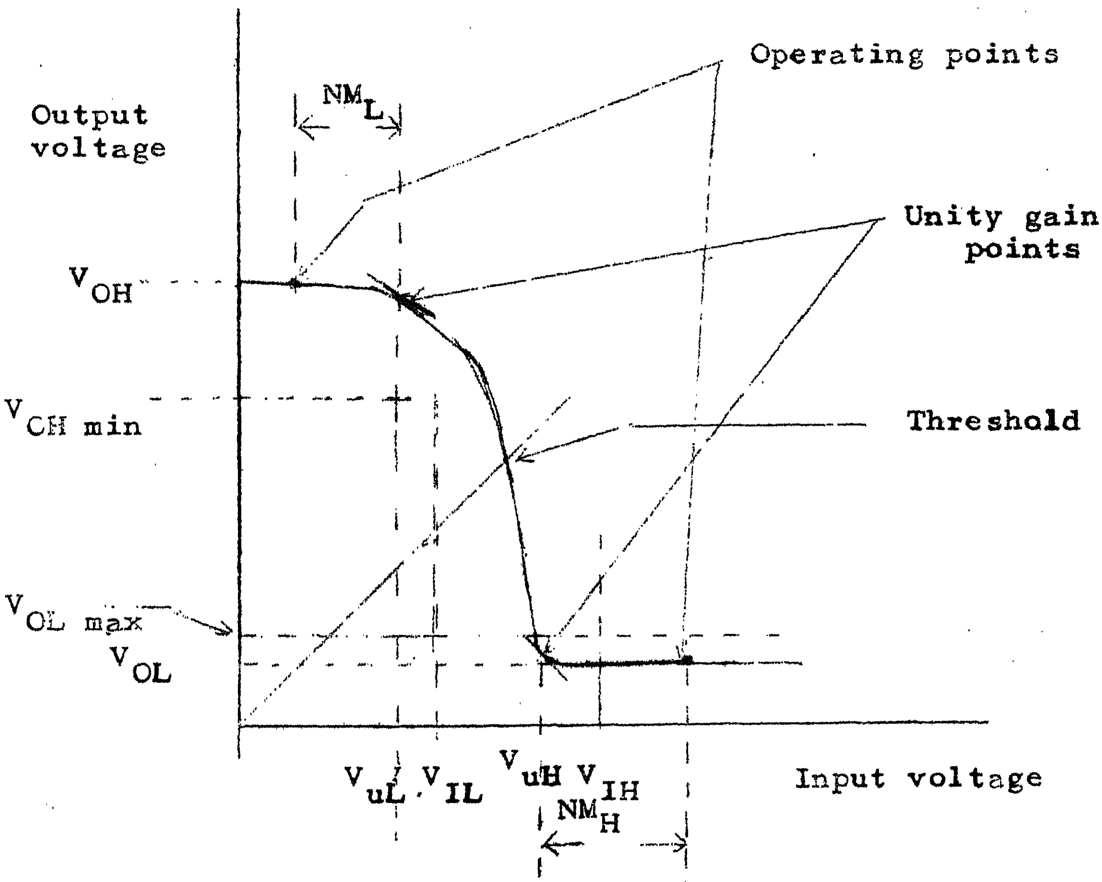



Fig. 2.1 Transfer Characteristic of an Inverter

### 2.4.1 Operating points

The two quiescent states in which the gate will rest when it is driven by and in turn drives similar gates are normally called the operating points, and are specified by the output voltage levels $V_{oL}$ and $V_{oH}$ in the extreme states where the output is low and high respecigely. These levels are never exactly $V_{cc}$ (the supply voltage) and O (GND), for any practical gate embedded in a system. These levels are functions of fan out, supply voltage and temperature. A gate must satisfy the worst case limits of $V_{oL}$ and $V_{oH}$ levels in order that it can be used reliably in a system.

### 2.4.2 Threshold

The threshold voltage ($V_t$) of a gate is recursively defined as that input voltage which yields the same output voltage. The threshold point is determined from the transfer characteristic by its intersection with a 45° line. The physical significance of the threshold voltage is that if the output voltage of any gate falls below $V_t$ the output voltage of the gate driven by the previous one will be above $V_t$, which in turn will force the following gate to have its output voltage below $V_t$ and so on. Hence the name threshold.

### 2.4.3 Unity gain points and Noise margins

Noise in a logic system is defined as any unwanted signals within the system. Noise can be classified as power supply noise, internally generated noise via cross talk or externally induced noise. Noise voltage may temporarily cause the logic circuit to change states, resulting in an erroneous output. Since noise is usually a random high frequency disturbance, it will be prevented from being amplified as long as the gate operates in the "flat" portions of the transfer characteristic. In order to obtain a definite measure of the noise suppression capability, one defines unity gains points as the two points on the transfer characteristic where the magnitude of the incremental gain of the gate is unity as indicated in Fig. 2.1.

The input noise margins are defined as those voltages corresponding to the horizontal distances from the operating points to the corresponding unity gain points. Thus low noise margin $NM_L = V_{uL} - V_{OL}$

and high noise margin $NM_H = V_{OH} - V_{uH}$

The interpretation for these high and low noise margins are as follows. These represent the maximum noise voltage that can be tolerated at the input of a gate in a system when it is in appropriate logic state, without the

possibility of the noise being amplified in the system.

## 2.5 FLIP-FLOP CHARACTERISTICS

Flip-flops are classified according to the type of clocking mechanism and according to their functions

Based on clock input flip-flops (FF) are classified as.

(a) D.C. or edge triggered FF inwhich - the clock causes FF operation at a particular voltage, when either a positive or a negative transition occurs only one transition being recognised for any device.

(b) A.C. coupled FF, inwhich the clock is capacitively coupled internally to the latching mechanism of the FF, leading to a high degree of dependence on the clock transition times.

(c) Master slave FF which consists of a master latch and a slave latch; the data being entered into the former at the leading edge of the clock, and transferred to the latter at the trailing edge.

Based on their function flip-flops are classified into three types.

(a) RS type flip flop which has two data inputs R and S, used for resetting and setting respectively, the flip flop states being unaffected or unpredictable according as both inputs are simultaneously low or high.

(b) JK type FF has two data inputs J and K essentially similar to S and R in the RS type, with the only difference that the Flip Flop toggles when both J & K are high.

(c) D type FF which has only one data input from which the data is entered by each clock pulse.

Besides the clocked data inputs referred to above most IC flip flops have asynchronous inputs, for example, clear and preset. Normally these asynchronous inputs which don't need clock input for their operation are over riding controls and have to be used carefully to avoid hazards.

Flip flops cannot normally be clocked while their inputs are changing, the transitions being prohibited for a certain interval of time known as set up time, prior to the appearance of the enabling edge of the clock. Set up time is of the order of 10 to 20 nano seconds for DC edge triggered flip flops and is equal to the clock pulse in the case of master-slave flip-flops.

## 2.6 TRANSIENT CHARACTERISTICS

Transient characteristic of gate circuits are specified by rise, fall and delay times. The definitions of these parameter are indicated in Fig. 2.2.

The rise and fall times are specified as those times necessary to traverse between 10% & 90% of the logic

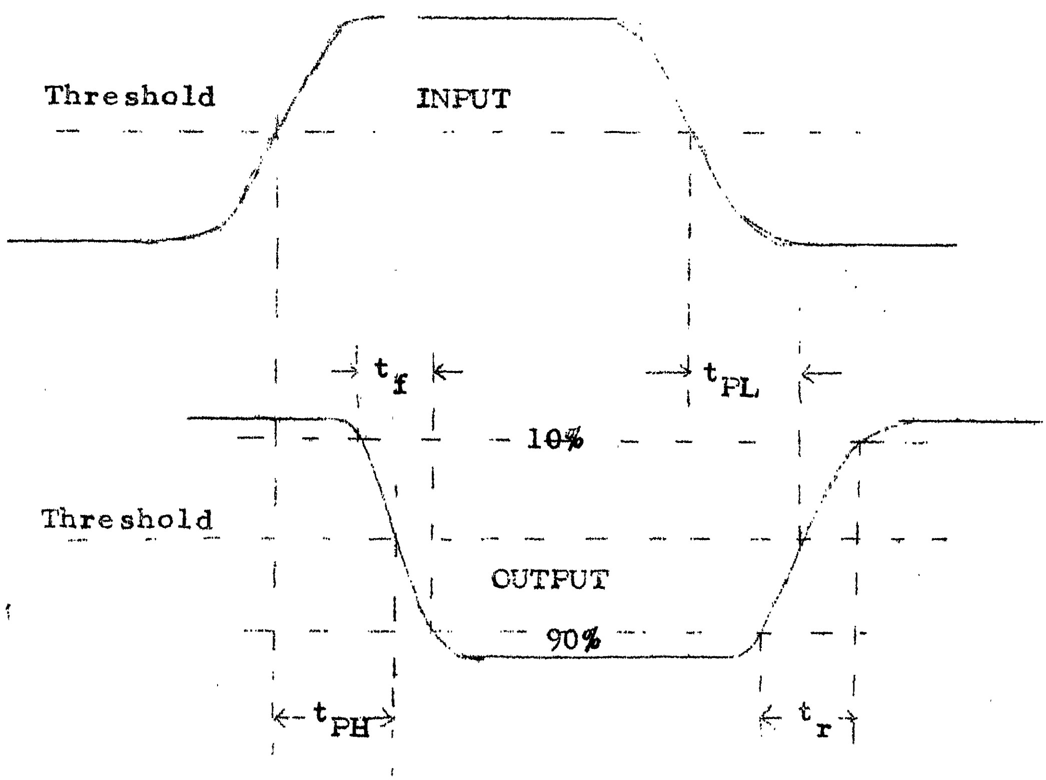



Fig. 2.2 Transient Characteristics

swing. Delay times are measured between the points where the waveform passes through the switching threshold. The delay time between a rising input and falling output is termed $t_{pH}$ and correspondingly the time between a falling input and rising output is termed $t_{pL}$. Another common way of specifying the delay of the gate is the pair delay which is equal to the sum $t_{pH} + t_{pL}$. The most important of the transient characteristics of a gate is the propagation delay, while for a bistable element, the speed may be specified either in terms of propagation delay between input and output or by the maximum continuous switching speed when it is driven by a train of clock pulses.

# CHAPTER-III

## TERMINOLOGY OF DIGITAL IC TESTING

### 3.1 MANUFACTURER'S AND USER'S POINTS OF VIEW

Having emphasised the need for testing in Chapter I, at this stage it is necessary to make a distinction between the IC user and the IC manufacturer. The manufacturer is under obligation to test and to see that the product meets his stated specifications. Infact each IC in the course of its travel from wafer to packaged device is often tested several times and each test involves the qualifications of many circuit functions and parameters. Also, the manufacturer can frequently use the results of such tests to monitor his production process. A lot to lot shift in the distinction of certain key parameters, for example, might alert him to a process change that, if undetected, could lead to costly field failure.

On the other hand, a user is under no such obligation to test the devices he uses. With the introduction of inregrated circuit logic elements, it is possible , at least for some class of users, to use these elements in much the same way as circuit engineers use electronic components. They can interconnect the basic

digital blocks available suitably to achieve their required output, without concerning much with the actual circuit of the logic element. Such class of users may be satisfied if the digital device performs according to the truth table for that device, within the stated specifications of the manufacturer.

On the other hand there may be other class of users who are interested in pushing the performance of the IC as far as possible or to extend their range of operation. For them the type of testing needed may be quite rigorous and depends on how the various parameters of the IC affect their circuit operation.

Based on these factors the tests on digital IC's are classified as:

1. Functional Tests
2. Parametric Tests
3. Dynamic or A.C. Tests.

## 3.2 FUNCTIONAL TESTING:

Functional Testing checks the logic operation of the digital IC's as defined by the truth table. For this purpose all possible combinations of 1's and 0's are applied to the inputs of Device Under Test (D.U.T.) & each output is checked to determine that it is in the proper logical state for the particular input combinations being applied. Precise measurements are not made; only logical

operation in accordance with the truth table is verified. Thus, for a complex device, functional testing may involve a large number of tests. An automatic tester must therefore perform functional testing of these devices at the highest possible speed. The number of such tests increases with the complexity of the digital IC. That is why exhaustive testing techniques on MOS/LSI IC's calling for patterns covering all possible combinations are often impracticable Considerable saving in time can be achieved by isolating the most probable failure modes of the device and then establishing a test sequence designed to detect these particular faults. Another approach is based on the application of random patterns to the inputs and the statistical probability that these will test the device adequately. Programming is important here because through software the test time can be optimized to reach an estimated level of probability of acceptable performance.

There are two basic types of digital logic circuits each of which requires a different test procedure. If the output logic states can always be defined exactly for all possible combinations of inputs, the circuit is called combinational. In this case there is a specific logic pattern output for any given input pattern, regardless of the order in which the input pattern is applied.

Sequential logic, on the other hand, has internal storage (flip-flops, latches and so forth). The logic pattern outputs of such circuits are functions of the input test pattern and also of their sequence.

In combinational logic, if there is an error in one pattern, it has no effect on the following outputs. But in sequential logic an error in a test pattern, or a noisy line that causes an internal element to change state may cause trouble. The sequence of output patterns may not be what it should, and good IC's may be rejected.

## 3.3 PARAMETRIC TESTING

Functional testing even when exhaustively complete, cannot be relied upon to determine whether the IC will operate in a desired application. The test system cannot simulate all possible circuits in which the device may be used and it is therefore necessary to measure certain parameters and compare them against specified limits. In parametric testing the DC or static parameters of the IC under test are measured. Such tests include measurements of forward and reverse currents, both at the input and output terminals, logic levels, noise margins and so forth. These measurements will define the fan-out capabilities of the device as well as leakage current, power dissipation etc.

The technique for making parameteric tests is to force a voltage or current at an input terminal and to compare the resulting output voltage or current against a limit. The test result can be taken as a simple GO/NO-GO indication or A/D conversion techniques can be applied to record the actual value of the parameter in question. One such technique is a software directed sequential approximation in which a series of GO/NO-GO comparisons are made, the reference converging to the unknown.

## 3.4 DYNAMIC TESTING

Dynamic testing checks such time dependent parameters as propagation delay, rise time, fall time etc. These tests are far more difficult, time consuming and expensive to perform than functional or parametric tests. Dynamic or ac testing requires special purpose equipment and circuitry (nano second pulse/pattern generators, test fixtures designed for high speed data handling etc.) Because of the high cost involved in the reliable performance of dynamic tests, these tests are performed only on a sample basis.

## 3.5 RELATIVE IMPORTANCE OF THESE TESTS

It is important to note that these three types of tests, namely, functional, parametric and dynamic are related to distinctly different properties of an IC and that a test

sequence of one type only, no matter how thorough, can not provide adequate device characterisation.

The usual pattern of testing digital IC's is to perform the functional testing first to find catastrophic failures caused by improper packaging bonding, metalization etc and parametric and dynamic tests to uncover failures due to surface or oxide effects. These tests have varying degrees of importance to IC manufacturers and IC users who may expect different degrees of performance from the device.

The functional testing is more useful from the user's point of view and parametric and dynamic testing are more useful to device manufacturers and also to users who want to use these devices under extreme conditions or to those who wish to extend the range of performance of these devices.

## 3.6 EMBEDDING OF THE D.U.T. IN AN AUTOMATIC TESTER

The flexibility of any automatic tester depends heavily on its capability of embedding different types of D.U.T. with a minimum amount of manual alteration in the various interconnections. Because of the great variety of digital devices in terms of inputs, outputs and the lack of standard pin connections for these devices, there is a strong need for identifying the inputs and outputs

of the D.U.T. for properly connecting sources and loads. This switching of device pins is the primary factor determing the overall testing speed of automatic testers. The various hardware techniques that can be used for this purpose are listed below.

1. The inter connection pattern between the device pins and the external circuit can be accomplished by some type of matrix. Usually slide switches, push buttons or thumbwheel switches are used for this purpose.

2. Alternatively, the user can use a patch board appropriately wired depending on the D.U.T. on hand, similar to that used in analog computers or in vaccuum tube testers to connect the device pins to power supply and enternal circuit. This scheme requires that the user must be aware of the pin connections of the D.U.T.

3. A third possiblity is to make use of electronic switching circuits for obtaining various desired interconnections. However, the undesirability of any impedance in any connecting path rules out the possibility of using electronic analog switches like transistors or FETs which have considerable ON resistance. Reed relays which have essentially zero ON resistance are often used. Some manufacturers use cross point matrices for making the required interconnections. Each cross point matrix is an array of digitally controlled dry reed relays and the

connections between measuring or input lines and pins may be made or broken in any preplanned sequence.

4. Finally, it is also possible to use the so-called hardware or printed card programming. The inputs, outputs and the power supply pins of the D.U.T. are brought out in a particular format to the terminals of a printed circuit card specially prepared for each type of device. The information about the type of the device e.g. gate or FF, the number of inputs and outputs, the loading information for that device are also coded in a particular format. This coding is essential for uniquely identifying the device for properly appling test conditions & connecting loads.

It is worthwhile at this stage to make a comparison of the various techniques discussed above.

The first two are essentially manual methods and are as such not compatible with any automatic test system. while the third and fourth are suitable for automatic testing. The third scheme can achieve a good reliability of connections and a relatively high speed; but its main disadvantage is the cost of reed relays which may be required in large numbers.

The last method discussed has the advantage of lower cost and a high degree of reliability . In this scheme the D.U.T. is mounted on the programmed printed

card, often referred to as the device card and is inserted in the test station and the user need not bother about the device pin numbers and their interconnection with external circuit. Hence this scheme is particularly suited for operation with unskilled operators. Of course the user must use the proper device card since the device card is unique for any device. Increase in the complexity of the device leads to a corresponding increase in the code necessary to uniquely identify the device, the complexity of the decoding circuit and the number of inputs and outputs and thereby places a limitation on this scheme.

For testing MOS/LSI devices which have considerably large number of inputs and outputs the concept of hardware programming is obviously ruled out. Testing of these devices require a long sequence of tests and each test scheme and test conditions may depend on the results of previous tests in the sequence. Hence testing of these devices can not be done without the use of a computer. In such cases interconnection of appropriate device pins to external circuit is achieved through software programming in which the inter connection can be made or broken in a preplanned sequence. Also it is possible with a change of program to accomodate different types of devices and newer circuits.

# CHAPTER - IV

## FUNCTIONAL TESTER DESIGN

As pointed out in the last Chapter, the functional IC tester is quite useful for quick inspection of incoming IC's, particularly in small scale industries and research institutions. Also it is necessary to make functional testing first, to find out whether the IC is good or not and then if necessary to go in for parametric or dynamic tests. Hence it has been decided to make this unit separate from the parametric test unit which is discussed in Chapter VI.

One way to perform functional testing is to compare the outputs of the D.U.T. with those of a reference unit having the same truth table as the D.U.T., both the units having the same chosen input pattern. Since using an external reference device for each one of the devices to be tested is not often convenient, all the more so if the tester is to be operated by relatively unskilled operators, it has been decided to generate the reference for each of the chosen set of devices in the instrument itself. The device is thus to be identified by an appropriate coding scheme, which will be described in the next section.

## 4.1 HARDWARE PROGRAMMING AND CODING SCHEME

Since we have restricted our testing to gates and flip-flops available in the 7400 series of TTL family, reasons given in the last chapter clearly indicate that the use of hardware programming is best suited for our purpose. This is done by making a printed circuit for each gate or flip-flop, belonging to this series, so that the input, output and power supply terminals of the D.U.T., are extended through the printed circuit, to the terminals of an edge connector, connected to the test system. We have chosen a 22-pin connector since this enables one to accommodate any digital circuit having upto 8 inputs and 4 outputs, 2 special inputs like clock, leaving 6 pins for the purpose of coding. It is easy to verify that any digital circuit having 8 inputs and 4 outputs can be appropriately coded for being tested by the proposed system. Evidently all gates and flip-flops belonging to the 7400 series form a subset of the above and can therefore be conveniently handled. Table 4-1 gives the general format of the pin connectors chosen for gates and flip-flop circuit cards.

TABLE 4.1

GENERAL PIN CONNECTION PLAN

| Pin No. | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Connection | | | | | | | | | | $0_1$ | $0_2$ | $0_3$ | $0_4$ | $Q_{CL}$ | – | A | B | C | D | E | F | |
| | GND | INPUTS | | | | | | | | OUTPUTS | | | | CLOCK | | CODES | | | | | | $V_{CC}$ |

It is advantageous, both from the point of view of speed and hardware requirements to test all gates/ flip-flops of a multiple IC simultaneously. The corresponding inputs of the different gates / flip-flops of multiple IC's are therefore brought out to the same input terminal of the connector, which then will be connected to independent input waveforms. If the D.U.T. has two independent inputs, these are brought out to first two terminals and if it has three independent inputs to first three input terminals etc. All outputs are brought out separately to as many pins as necessary among pins 10-13. Pin number 1 is used for Ground and pin number 22 for power supply $V_{CC}$

The necessary information about the D.U.T. and the coding scheme for these are given in Table 4.2.

TABLE 4.2

CODING SCHEME

| Information | | | Coding |
|---|---|---|---|
| Device Identification | | Inverter | A = 1 |
| | | Gate | B = 0 |
| | | Flip-flop | B = 1 |
| Gate Type | Logic | NOR | C = 0 |
| | | NAND | C = 1 |
| | Input Output | Quad 2-input | D = 0 E = 0 |
| | | Triple 3-input | D = 0 E = 1 |
| | | Dual 4-input | D = 1 E = 0 |
| | | Single 8-input | D = 1 E = 1 |
| Flip-flop Type | Clocking Method | DC Edge triggered | C = 0 |
| | | Master-Slave | C = 1 |
| | Input | RS | D = 0 E = 1 |
| | | JK | D = 1 E = 1 |
| | | D | D = 1 E = 0 |
| Fan out | | 10 | F = 1 |
| | | 30 | F = 0 |

## 4.2 SYSTEM DESCRIPTION

A simplified block diagram of the scheme is shown in Fig. 4.1. The instrument mainly consists of 3 blocks.

1. The Pattern Generator: All possible 8-bit combinations of 0 and 1 to be applied as the inputs of the D.U.T. are generated by this unit. The same pattern is also used for generating the reference outputs.

2. The Reference Generator: Depending upon the code as contained in the circuit card, this unit is programmed to generate the same input-output relationship as that expected of the D.U.T.

3. Comparator and Indicator unit: A digital (binary) comparator is used to compare the output (s) of the D.U.T. with the reference outputs. Any error is used to set the corresponding Error Latch, which turns on the corresponding reject lamp to indicate failure. It should be noted that each reject lamp indicates the failure of a particular <u>output</u> and the failure or other-wise of a gate/flip flop in the D.U.T. is to be properly interpreted from the knowledge of the exact scheme used for interconnecting the device outputs and the output terminals of the circuit card.

The design of these blocks are discussed in the following sections.

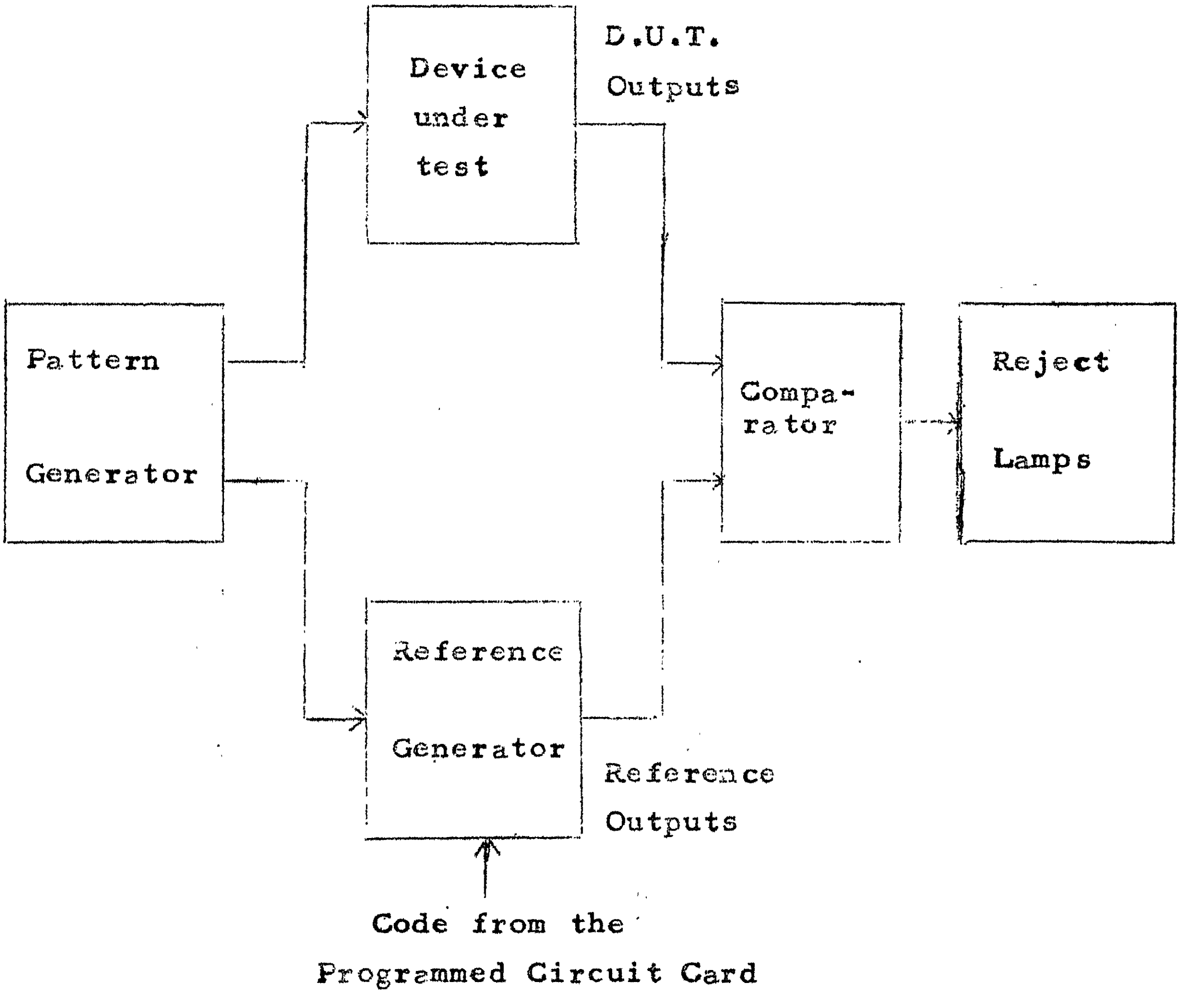



Fig. 4.1 Block Diagram of the Functional Tester.

## 4.3 PATTERN GENERATOR

To obtain inputs having all possible 8 bit combinations of 0 and 1, the simplest method is to divide a square wave by 8 flip-flops in cascade and to make use the outputs of these flip-flops as the eight inputs. An eight stage synchronous ripple carry counter has been designed for this purpose using conventional methods[4]. The square wave generator for this purpose is chosen to have a frequency of 10 KHz, from the considerations of test speed and hardware limitations. As pointed out in Chapter I, high test speeds alone, without the use of automatic handling facilities, cannot provide high speed of testing and as such, a frequency above 10 KHz would give no speed advantage at all, while creating some hardware problems.

## 4.4 REFERENCE GENERATOR FOR GATES

An eight input gate is chosen and its inputs are appropriately generated depending on the code, as contained in the circuit card. The output of this gate or its complement is obtained as reference output for gates. For NAND gates the inputs that are applied to the D.U.T. are also applied to the 8-input gate, the output of this gate being the reference output.

For testing NOR gates De Morgan's theorem is made use of. The inputs to the 8-input gate clearly have to be the complements of the inputs applied to the D.U.T., and

the reference output is then the complement of the output of the 8 input gate.

The logical expressions for the eight inputs denoted by $I_1$, $I_2$..............$I_8$ are easily seen to be given as follows, in terms of the codes defined in section 4.1

$$I_1 = C \oplus \bar{Q}_{P1}$$

$$I_2 = C \oplus \bar{Q}_{P2}$$

$$I_3 = \overline{(C \oplus Q_{P3})\ \overline{\bar{D}.\bar{E}}}$$

$$I_4 = \overline{(C \oplus Q_{P4}).D}$$

$$I_5 = \overline{(C \oplus Q_{P5}).D.E}$$

$$I_6 = \overline{(C \oplus Q_{P6}).D.E}$$

$$I_7 = \overline{(C \oplus Q_{P7}).D.E}$$

$$I_8 = \overline{(C \oplus Q_{P8}).D.E}$$

where $Q_{P1}$, $Q_{P2}$ ........$Q_{P8}$ are the eight outputs of the pattern generator.

## 4.5 REFERENCE GENERATOR FOR FLIP-FLOPS

The basic distinction between the schemes for generating the reference outputs for gates and flip-flops arises from the existance of two kinds of inputs synchronous and asynchronous, for the latter.

In the case of gates, the code available from the circuit card has been used to generate the inputs of an 8-input gate, whose output determines the reference outputs. But in the case of flip-flops it is not practicable to generate the reference outputs by controlling the inputs of a single flip-flop of any chosen type, because of the following reasons:

1) Flip-flops have widely different characteristics in terms of asynchronous modes of operation and hence the hardware requirements for controlling the inputs to get the desired output is quite large.

2) The use of a single flip-flop for generating the reference outputs is not always reliable due to the sensitivity of flip-flops to noise in the system.

Hence it has been decided to design separate combinational circuits to generate the outputs corresponding to each type of flip-flops to be tested. The codes are used to select the appropriate outputs from these as the reference outputs.

If at the enabling edge of the clock, any of the asynchronous inputs change, the output state of the flip-flop after clocking may be unpredictable. To take care of set up time specifications, the clock to be applied to the test flip-flop should be such that all the other inputs are stabilized before and after the

application of the clock. This is conveniently done by ANDing $Q_A$ and $\bar{Q}_B$ , where $Q_A$ and $Q_B$ are obtained by dividing the square wave from the basic astable, as shown in Fig. 4.2.

The eight output signals of the Pattern Generator are generated by successive frequency division of the $Q_B$ waveform, as already pointed out in section 4.3. This therefore ensures that none of the inputs has any transition during the transitions of the clock and also when the clock is high.

A simple method of testing flip-flops is to treat asynchronous inputs just as any other synchronous inputs only ensuring that the enabling edge of the clock does not interfere with any edge of asynchronous inputs. The expected outputs Q and $\bar{Q}$ of the flip-flop are generated combinationally. Since the asynchronous inputs always have overriding control over the synchronous inputs, obviously, choosing the slowest of the eight outputs coming from the Pattern Generator for these will result in simpler hardware to generate the expected outputs.

In this method, it is possible that some of the transitions of the flip-flop may not be tested at all. Another scheme in which all possible transitions of the flip-flop will be tested is to apply all combinations of synchronous inputs for each initial state of the flip-flop.

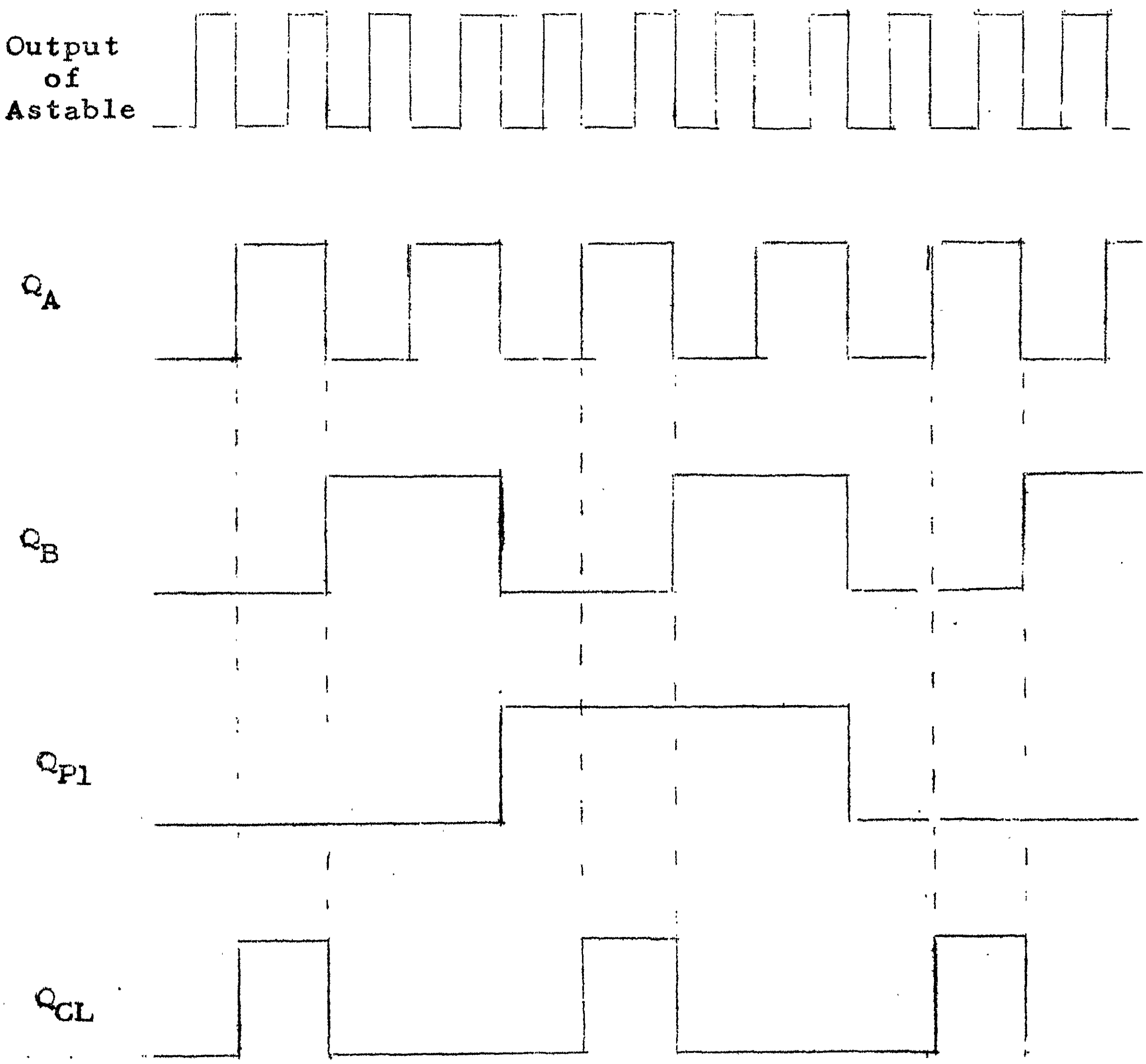



Fig. 4.2 Clock Waveform of the Flip-flop under test

This is done by bringing the flip-flop to one or the other of the two possible initial states every time before the clock pulse is applied. However,it is highly improbable that a flip-flop which passes the testing by first scheme will fail in the other scheme.

The first scheme is made use of in our present system. The logical design for generating the reference outputs for two specific types of flip-flops ( SN 7473 and SN 7474) using the second scheme is given in Appendix IV.

## 4.6 LOGICAL DESIGN FOR INDIVIDUAL FLIP-FLOPS

As pointed out in the last section, each flip-flop to be tested requires that reference outputs (Q and $\overline{Q}$ ) corresponding to this flip-flop be generated.
Hence it has been decided to test only the most commonly available flip-flops at present. These are

(1) Master slave JK flip-flop (SN 7473)

(2) Edge triggered D flip-flop (SN 7474)

(3) DC clocked JK flip-flop (SN 7470)

The logical design for generating the expected outputs of each one of the above flip-flops is given below:

### 4.6.1 Master Slave JK Flip-flop (SN 7473)

The $Q_{P1}$, $Q_{P2}$, $Q_{P3}$ outputs from the Pattern Generator are applied to J,K, $R_D$ inputs of the flip-flop under test respectively. It is easily seen from

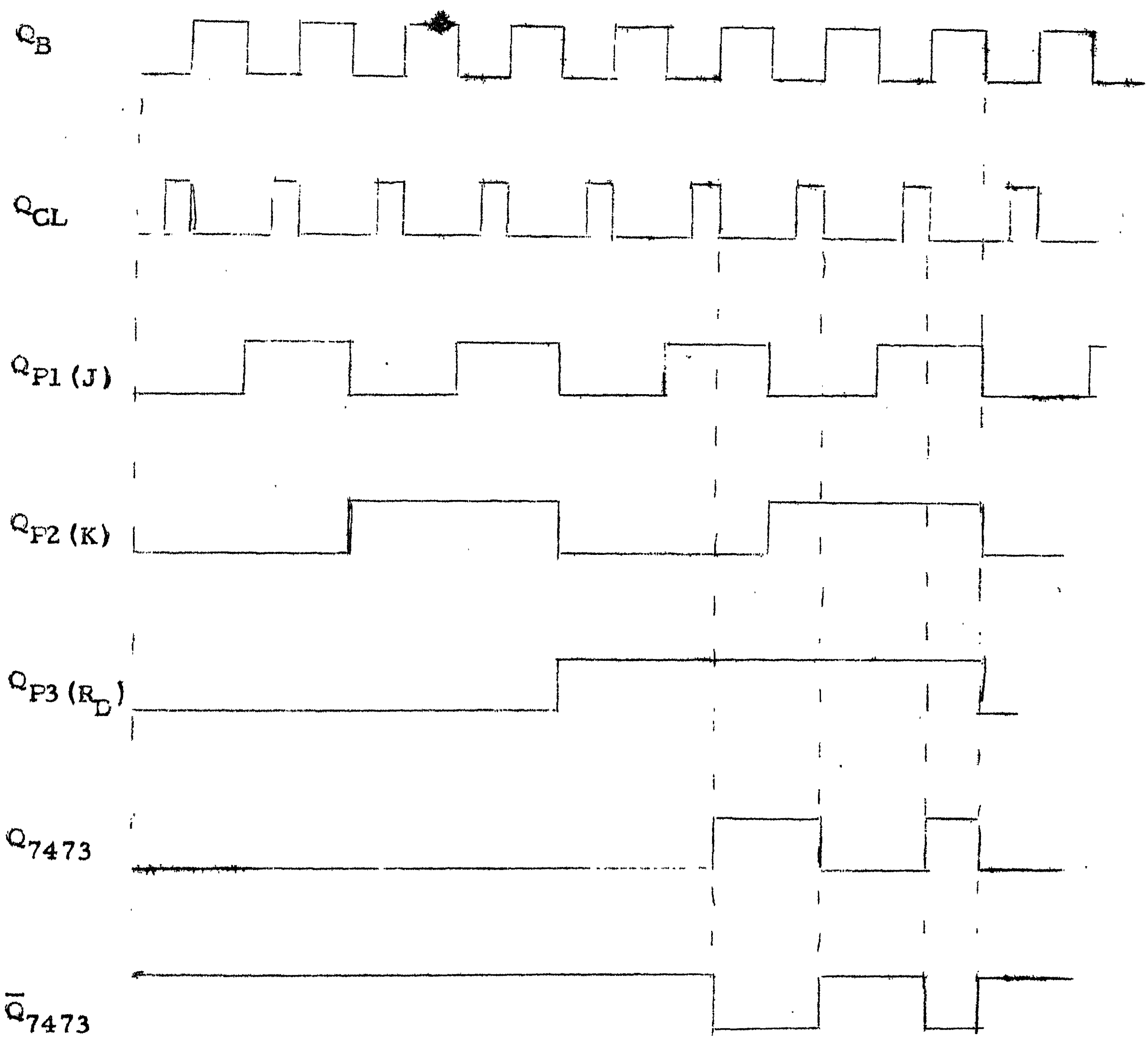



Fig. 4.3 Expected outputs for Master Slave JK Flip-flop (SN7473)

Fig. 4.3 that the expected Q and $\overline{Q}$ outputs are given by

$$\text{Expected Q output } Q_{7473} = Q_{P3}(Q_B \cdot Q_{P1} + Q_B \cdot Q_{P1} \cdot Q_{P2}) \qquad (IV.1)$$

$$\text{Expected } \overline{Q} \text{ output } \overline{Q}_{7473} = \overline{Q_{7473}} \qquad (IV.2)$$

### 4.6.2 Edge Triggered D Type Flip-flop (SN 7474)

The D, $R_D$, $S_D$ inputs of the flip-flop are connected to $Q_{P1}$, $Q_{P2}$, $Q_{P3}$ respectively. It is clear from Fig. 4.4 that the expected Q & $\overline{Q}$ outputs to be.

$$\text{Expected Q output } Q_{7474} = \overline{Q_{P3}} + Q_{P2}\, Q_{P1}\,\overline{(\overline{Q}_A \cdot \overline{Q}_B\ )} \qquad (IV.3)$$

$$\text{Expected } \overline{Q} \text{ output } \overline{Q}_{7474} = Q_{7474} + Q_{P2} \cdot Q_{P3} \qquad (IV.4)$$

### 4.6.3 DC Clocked JK Flip-flop (SN 7470)

The inputs $Q_{P1}$ $Q_{P2}$ ............$Q_{P6}$ are applied to $J_1$, $J_2$, $K_1$, $K_2$, $J^*$ , $K^*$ inputs of the flip-flop respectively. The asynchronous inputs are not tested in this scheme. For the six synchronous inputs $2^6 = 64$ combinations are possible and 64 clock pulses are needed to test for all combinations of inputs. These combinations are labelled by numbers 0,1... ------ 64 where 0 corresponds to $\overline{Q}_{P6} \cdot \overline{Q}_{P5} \cdot \overline{Q}_{P4} \cdot \overline{Q}_{P3} \cdot \overline{Q}_{P2} \cdot \overline{Q}_{P1}$ and 1 to $\overline{Q}_{P6} \cdot \overline{Q}_{P5} \cdot \overline{Q}_{P4} \cdot \overline{Q}_{P3} \cdot \overline{Q}_{P2} \cdot Q_{P1}$ and so on. Since the effective J input is given by

$J = J_1 \cdot J_2 \cdot J^*$ we have

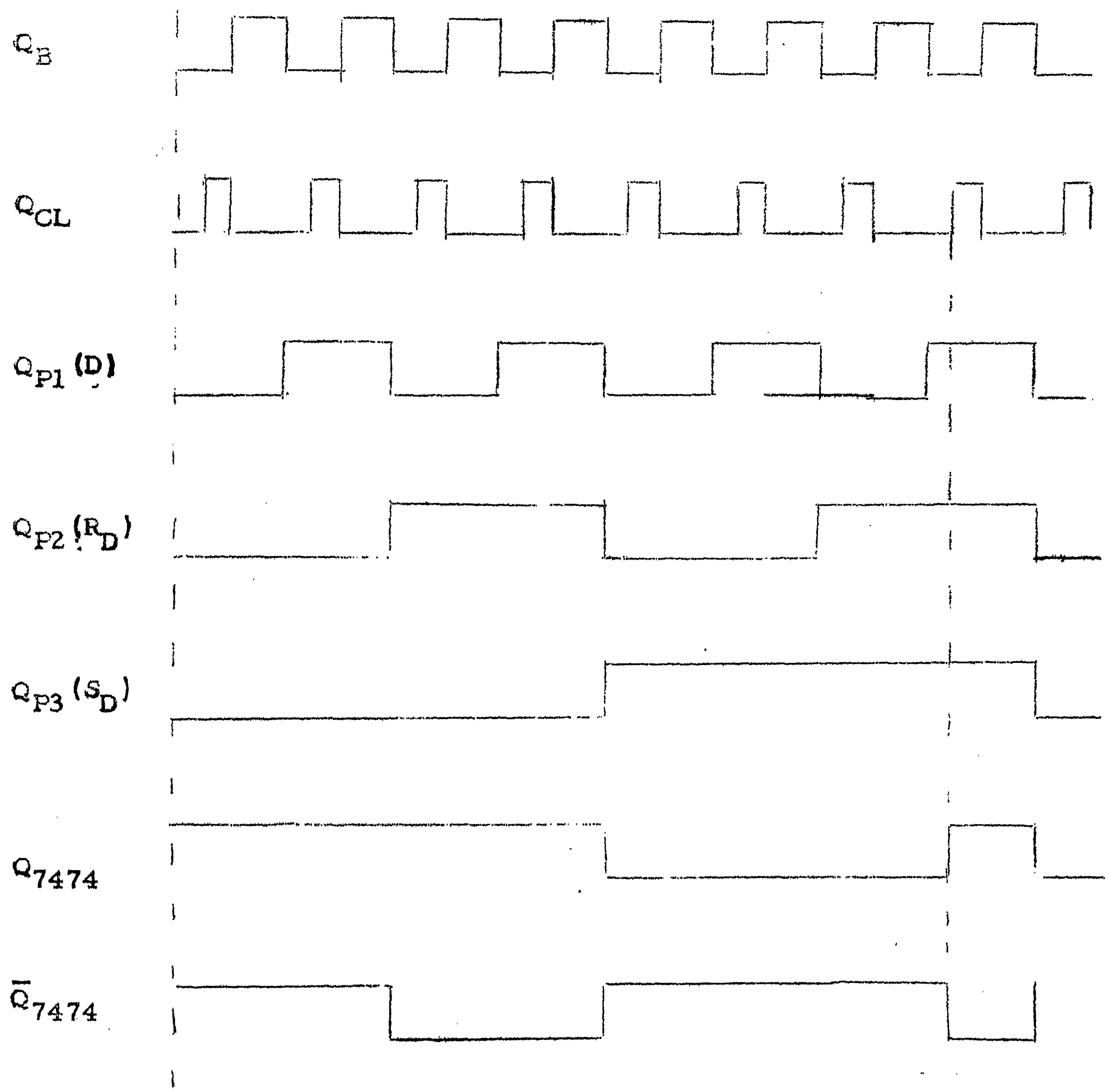



Fig. 4.4 Expected outputs for
Edge triggered D Flip-flop (SN7474)

$$J = Q_{P1} \cdot Q_{P2} \cdot \overline{Q}_{P5} \qquad (IV.5)$$

Similarly we have

$$K = Q_{P3} \cdot Q_{P4} \cdot \overline{Q}_{P6} \qquad (IV.6)$$

It is easily seen that

J = 1 for input combinations 3,7,11,15,35,39,43,47

and that

K = 1 for input combinations 12,13,14,15,28,29,30,31.

The following table gives the combinations of inputs at which flip-flop change of state occurs.

TABLE 4.3

OUTPUT CHANGES IN FLIP-FLOP SN 7470

| Combination No. | ACTION | STATE CHANGE | |
|---|---|---|---|
| | | FROM | TO |
| 11 | Reset | 1 | 0 |
| 15 | Toggle | 0 | 1 |
| 28 | Reset | 1 | 0 |
| 35 | Set | 0 | 1 |

It can be easily verified that the output of the flip-flop remains at 0 from the enabling edge of the 11th to that of the 15th clock pulse and from the enabling edge of the 28th to that of the 35th clock. The logical expressions for the output is given by

Expected Output $Q_{7470} = \overline{P_1 + P_2}$ where (IV.7)

$$P_1 = \overline{Q}_{P6}\cdot\overline{Q}_{P5}\cdot Q_{P4}\cdot Q_{P3}\cdot\overline{X}\cdot\overline{Y} \quad \text{and} \qquad \text{(IV.8)}$$

$$P_2 = \overline{Q}_{P6}\cdot Q_{P5}\cdot Q_{P4}\cdot Q_{P3}\cdot\overline{Y} + Q_{P6}\cdot\overline{Q}_{P5}\cdot\overline{Q}_{P4}\cdot\overline{Q}_{P3}\cdot\overline{X} \qquad \text{(IV.9)}$$

where $P_1$ and $P_2$ are the output $\overline{Q}$ waveform of the flip-flop between clock pulses 11-15 and between clock pulses 28-35 respectively and X and Y are given by

1 $$X = \overline{(\overline{Q}_A\cdot\overline{Q}_B)}\; Q_{P2}\cdot Q_{P1} \qquad \text{(IV.10)}$$

$$Y = \overline{Q}_A\cdot\overline{Q}_B\cdot\overline{Q}_{P1}\cdot\overline{Q}_{P2} \qquad \text{(IV.11)}$$

Simplifying the logic we get

Expected Q output, $Q_{7470}$ is given by

$$Q_{7470} = \overline{Q}_{P6}\cdot Q_{P4}\cdot Q_{P3}\cdot\overline{Y}\;\overline{(\overline{Q}_{P5}\cdot X)}$$
$$+\, Q_{P6}\cdot\overline{Q}_{P5}\cdot\overline{Q}_{P4}\cdot\overline{Q}_{P3}\cdot X \qquad \text{(IV.12)}$$

Expected $\overline{Q}$ output, $\overline{Q}_{7470} = \overline{Q_{7470}}$ (IV.13)

## 4.7 COMPARATOR

An exclusive-OR circuit is used as the binary comparator. Four such comparators are made use of, one for each output. If at any instant the D.U.T. output and the reference output do not match, output of the exclusive-OR gate goes high and sets the corresponding Error Latch.

It is sometimes necessary to inhibit certain latches from setting; for example, when testing an IC with a single output all the other Error Latches are to be inhibited or prevented from being set.

4.8 REFERENCE SELECTOR

In the present scheme, for all gates there is only one reference output, generated in accordance with the code for the D.U.T. On the other hand, for each of the three flip-flops that has been selected for testing, a pair of expected outputs ( Q and $\overline{Q}$ ) are available. Clearly, it is also desirable from the point of view of the user, to be able to use externally generated reference outputs in case the D.U.T. is not one of those types for which reference outputs are internally generated. This provision is therefore incorporated in the instrument with a manual selector switch, whereby the reference outputs may be chosen to be either INT(ernal) or EXT(ernal). With the selector switch in INT position, the appropirate reference output(s) is (are) chosen by logic circuits, according to the code available from the circuit card. Thus for any NAND/NOR gate of the SN 7400 series, the internally generated reference is selected and applied in parallel to the inputs of all four comparators; while for each of the three chosen flip-flops SN 7470, SN 7473 and SN 7474 the corresponding Q and $\overline{Q}$ reference outputs

are selected and applied pair wise to the inputs of the four comparators.

## 4.9 DESCRIPTION OF PANEL AND LAYOUT OF THE INSTRUMENT

The entire circuit of the instrument is spread over eleven printed cards . The function of each of these cards is indicated in Table 4.4. The D.U.T. is to placed in the appropriate circuit card which is inserted into a 22 pin connector. All the inputs of the comparators are brought out to the front panel, $0_1$, $0_2$, $0_3$, $0_4$ being the device outputs and $R_1$, $R_2$, $R_3$, $R_4$ being the reference outputs. The outputs of the Pattern Generator $Q_{P1}$, $Q_{P2}$,......$Q_{P8}$ are also brought out to the front panel terminals $P_1$, $P_2$ .........$P_8$. If it is desired to use external reference outputs these can be fed to terminals $R_1$,$R_2$, $R_3$, $R_4$.

Open collector gates require the connection of external pull up resistors from the outputs of the gates to the power supply. Also it may be necessary to carryout functional testing under various fan out conditions, by connecting suitable resistances from the output terminals to either power supply or Ground terminals. In order to do this, power supply and Ground terminals are provided on either side of the output terminals.

A patch board is also available in order that a skilled user can program the instrument in any manner desired

TABLE 4.4

CARD DESCRIPTION

| No | CARD | FUNCTION | |
|---|---|---|---|
| 1 | CARD A | Gated Astable and Clock Generator for DUT | |
| 2 | CARD B | 8-bit Synchronous Ripple Carry Counter (Input Pattern Generator) | |
| 3 | CARD C | GATE | Logic for Inputs $I_1$-$I_4$ of the 8 input gate (Ref. Card F) |
| 4 | CARD D | Reference | Logic for inputs $I_5$-$I_8$ of the 8 input gate (Ref. Card F) |
| 5 | CARD E | Generator | Final Stage of Gate Reference Generator in Corporating an 8-input gate |
| 6 | CARD F | Reference | Reference Generator for Q & $\overline{Q}$ Outputs of SN 7473 and SN 7474 |
| 7 | CARD G | Generator For Flip-flop | Reference Generator for Q & $\overline{Q}$ outputs of SN 7470 |
| 8 | CARD H | Reference Selector | |
| 9 | CARD J | Comparators and Error Latches | |
| 10 | CARD K | Reject Lamp Drivers | |
| 11 | CARD L | Regulator for Power Supply | |

Reject lamps $L_1, L_2, L_3, L_4$ correspond to D.U.T. outputs $0_1, 0_2, 0_3 . 0_4$ respectively, ordered according to the pin ordering in the circuit card connector.(Ref Table 4.II).

The clear push button (CLR) is used to reset all Error Latches, and all flip-flops.

The testing is started by pressing the start button. The instructions for operating the instrument is given in Appendix III.

## CHAPTER V

## PRINCIPLE OF AUTOMATIC PARAMETRIC TESTING

The motivation for the parametric testing and its relative importance to the IC user and the IC manufacturer has been discussed in chapter III. These considerations clearly indicate that, while functional testing can and is often done on any logic circuit, ranging from a simple gate to sub systems; parametric testing is relevent only for the basic inverter of the family since information about the inverter completely determines the static parameters of any other member of the same logic family. Some of the parameters of the basic inverter particularly those which could distinctly establish the acceptable limits are given below.

1. Logic levels ($V_{OL}$ & $V_{OH}$)
2. Unity gain points ($V_{uL}$ & $V_{uH}$)
3. Threshold ($V_t$)
4. Input currents ($I_{iL}$ & $I_{iH}$)
5. Power supply currents ( $I_{CCL}$ & $I_{CCH}$)

We are in the present work, concerned only with fast automatic GO/NO-GO type of testing, for which the testing method may be completely different from the manual method used in the laboratory for testing the same parameter.

There are two approaches to GO/NO-GO type of parametric testing. In one, the actual value of the parameter is measured and compared against limits to produce a GO/NO-GO result. On the other hand some times it is sufficient to check whether the outputs of the D.U.T. are within the expected limits or not when the input is also within a specified range. For example, in logic levels test of an inverter it may be sufficient to check for input voltage within the logic 0 range whether the output voltage is within the logic 1 range or not.

It is evident that the same printted circuit card as described in section 4.1 for functional testing can be used, with the same advantages for embedding the D.U.T. in an automatic set up for parametric testing. The same coding scheme used in the Functional Tester can be used for parametric testing also. But in the case of parametric testing it is essential to test logical inverters which are available six in a IC chip.Hence six output connections are required in the circuit card. The same pin connection scheme can be used for parametric tester also with the only difference that pin numbers 10 through 15 correspond to outputs in this case

5.1 SWEPT-INPUT TESTING

Testing of many of the parameters given above can be simpler if the input voltage is swept through its entire

range, sothat a continuous sequence of measurements can be made at both input and output of the device at all states of the device. Also it is possible that all the tests can be done in a single sweep. Hence it is clear that a ramp voltage waveform is best suited as input of the device, particularly in an automatic testing set up. Also choosing the ramp voltage as input has the advantage that the output of the inverter describes the transfer characteristics and makes the testing of certain parameters like threshold, unity gain points simpler.

As pointed out in Chapter II, it is essential to carryout many of the tests under various fan out conditions, sothat the testing conditions correspond to actual operating conditions. Hence even though all the parameters can be tested in a single sweep, it is necessary to use a repetitive ramp as input waveform sothat after every sweep the test can be carried out for a different fan out. Since a sharp fly back of a sawtooth input might cause oscillation problem when the inverter is between its extreme stable states a ramp voltage waveform with different slopes for rising and falling portions has been chosen as input waveform.

## 5.2 SEQUENCING OF TESTS

When the repetitive ramp voltage waveform is applied to the input, the output voltage of the D.U.T. is compared against expected values to produce a GO/NO-GO result. In one period of the input waveform all the tests are performed, unlike other testing methods in which the tests are conducted sequentially one after the other.

Though parametric testing on basic inverter of the family is sufficient it is some times desirable to test any multiple, multi-input NAND/NOR gate chip. Of course while testing one input, the other inputs should be disabled . An input selector is therefore necessary to select the appropriate input to be tested and for disabling the other inputs of the same gate.

These considerations indicate the need for a three-fold sequencing of tests. First the tests are to be carried out on an input for all fan outs. These tests are to be carried out on all such inputs of the gate and finally the same sequence to be repeated for all gates in the chip. It is obvious that three counters are necessary for this purpose, one labelled Input Counter for storing the information about which input is being tested at any time & another counter labelled Gate Counter for carrying out these tests on different gates of the chip

one at a time. The Fan Out Counter is necessary to contain the fan out count.

Intially all counters are cleared and input 1 of gate 1 is tested first, with zero fan out. During one cycle of the input sweep all the tests are performed on a gate input and at the end of this cycle the Fan Out Counter is incremented by one. This is repeated till the maximum fan out specified for that device, as found in the circuit card, is reached. Thus after testing a gate input for all fan outs the next input of the same gate if any, is tested, again for all fan outs.

After the maximum number of inputs is reached, the next gate of the chip if any,is tested; this time for all inputs and for all fan outs. An output selector selects the required output depending upon the gate count. When all the gates are tested a TEST OVER signal is generated.

When one input of a gate is being tested, the other inputs of the same gate are driven to appropriate logic states, usually the worst case limits. For NAND gates this level is $V_{OH\ min}$ and for NOR gates this level is $V_{OL\ max}$. In case of failure of any test/tests, this failure information is stored in a latch to turn on appropriate reject lamps.

## 5.3 FORCED CURRENT LOADING

In order that the test conditions correspond to actual operating conditions , it is necessary to carryout the parametric testing under various fan out conditions. Hence the requirement to test, with D.U.T. actually sourcing or sinking (depending on its state) all values of current commensurate with the entire permissible range of fan out. To achieve this, one possibility is to use gates of the same family as loads, the main difficulty in this method being different gate inputs are to be connected for various fan out and at the same time, without introducing any resistance in the connecting path. Usually the switching of fan outs is done at relatively high speed and hence the use of reed relays for this purpose is ruled out.

An easier alternative for this is to force appropriate currents into or out of the D.U.T, the magnitude of the current being determined by the fan out and the direction of the current by the output state of the D.U.T. Hence a bi-directional current source which can source or sink the required current, essentially in steps for successive fan outs is required.

Another requirement is that it should be able to source or sink currents of different orders of magnitude and must be able to change the direction at the appropriate time to take care of the safety of the D.U.T.

## 5.4 LOGIC LEVEL TESTS

Usually the logic 1 level is specified by $V_{OHmin}$, the minimum permissible output voltage level for logical 1, when the input voltage is less than or equal to $V_{IL}$ (Ref.sec. 2.4.1). The logic 0 level is specified by $V_{OL\ max}$, the maximum permissible output voltage level for logical 0, when the input voltage is equal to or more than $V_{IH}$ (Ref. sec. 2.4.1). As pointed out earlier, these levels are functions of fan out and temperature and hence it is necessary to carry out these tests under various fan out conditions.

### 5.4.1 $V_{OH}$ Test

In the present scheme of swept input testing, it is simpler to check these specifications than to actually measure and compare them with limits for a GO/NO-GO result.

As such in this test we are only interested in finding out for input voltages of the gate, less than or equal to $V_{IL}$, the set value, whether the output voltage is more than the expected value of $V_{OH}$ or not.

The input voltage applied to the D.U.T. is compared with the set value of $V_{IL}$ in a comparator whose output (A) is high as long as the input of the D.U.T. is less than $V_{IL}$. The output voltage of the D.U.T. is compared with the expected value of $V_{OH}$ in another

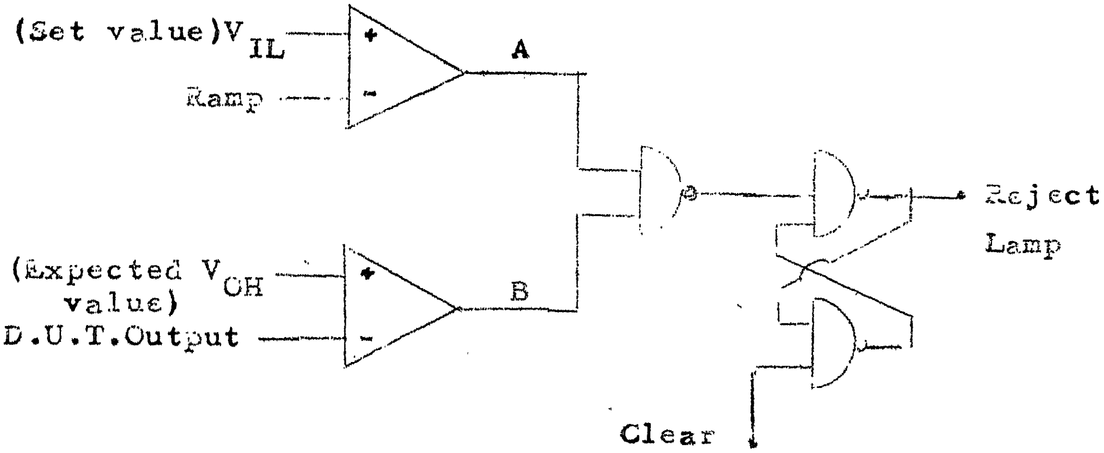



Fig. 5.1(a) $V_{OH}$ Test-scheme

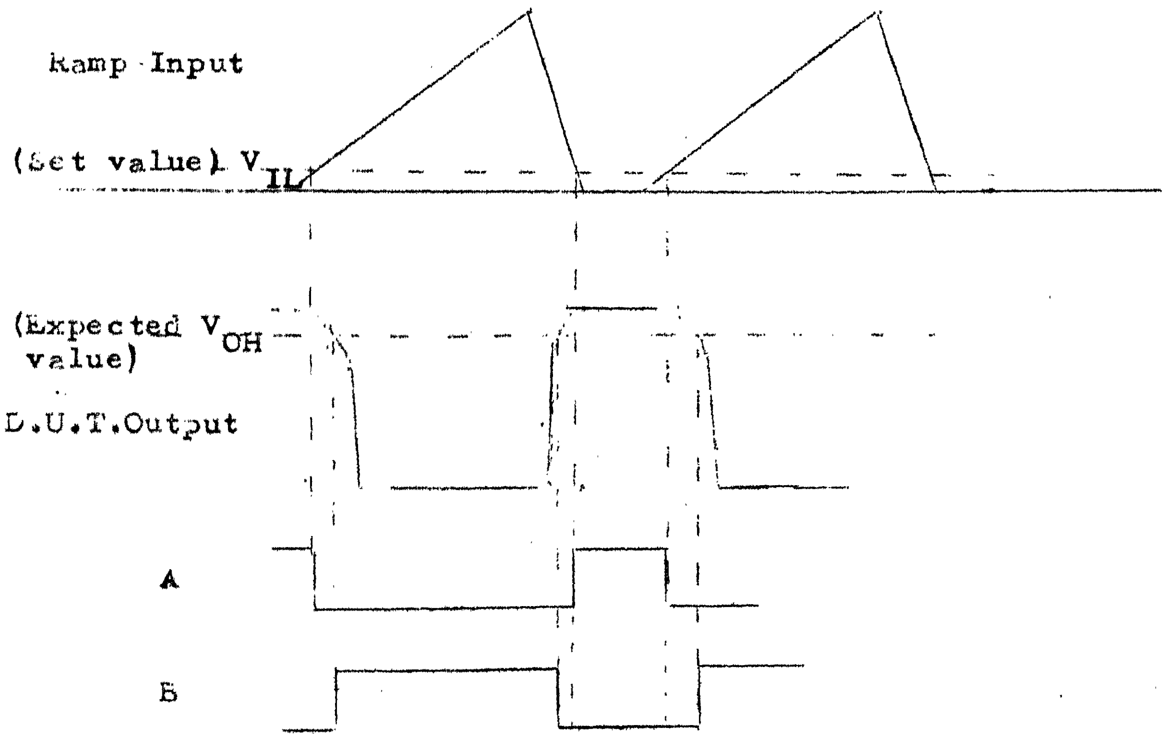



Fig. 5.1(b) $V_{OH}$ Test-waveforms

comparator, the output of which (B) is low as long as the D.U.T. output voltage is more than the other input of the comparator. For a gate to pass this test, the requirement is that both the outputs of the comparators should never be high. The failure condition is detected by NANDing the outputs of the comparator. If at any time the output of this NAND gate is low, the corresponding Error Latch is set and a reject lamp is turned on. The scheme of testing this parameter and the waveforms are given in Fig. 5.1(a) and Fig. 5.1(b) respectively .

### 5.4.2 $V_{OL}$ Test

The aim of this test is to find out for input voltages equal to or more than the set value $V_{IH}$, whether the output voltage of the D.U.T. is less than the expected value of $V_{OL}$ or not. Two comparators are made use of in this scheme also as shown in Fig. 5.2(a). The inputs to the first comparator being the ramp applied to the D.U.T. and the set value of $V_{IH}$ while the inputs to the second comparator being the D.U.T. output voltage and the expected value of $V_{OL}$.

It is clear from Fig. 5.2(b) that the output of the first compartor(C) is high if the ramp voltage is more than set value of $V_{IH}$ and that the output of the second comparator (D) is low as long as the D.U.T. output voltage is less than the expected value of $V_{OL}$. The requirement

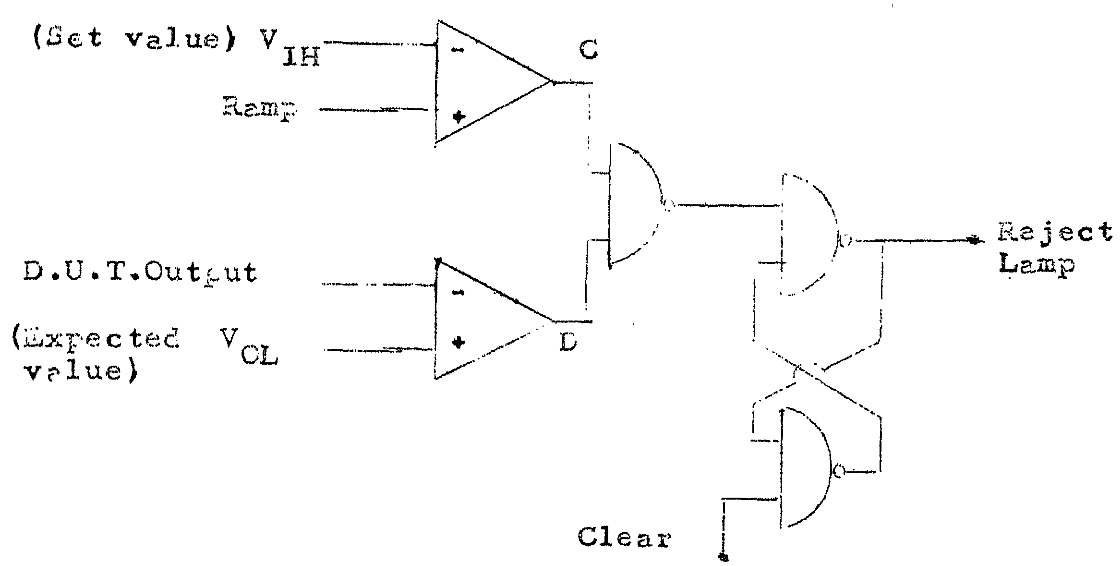



Fig. 5.2(a) $V_{OL}$ Test scheme

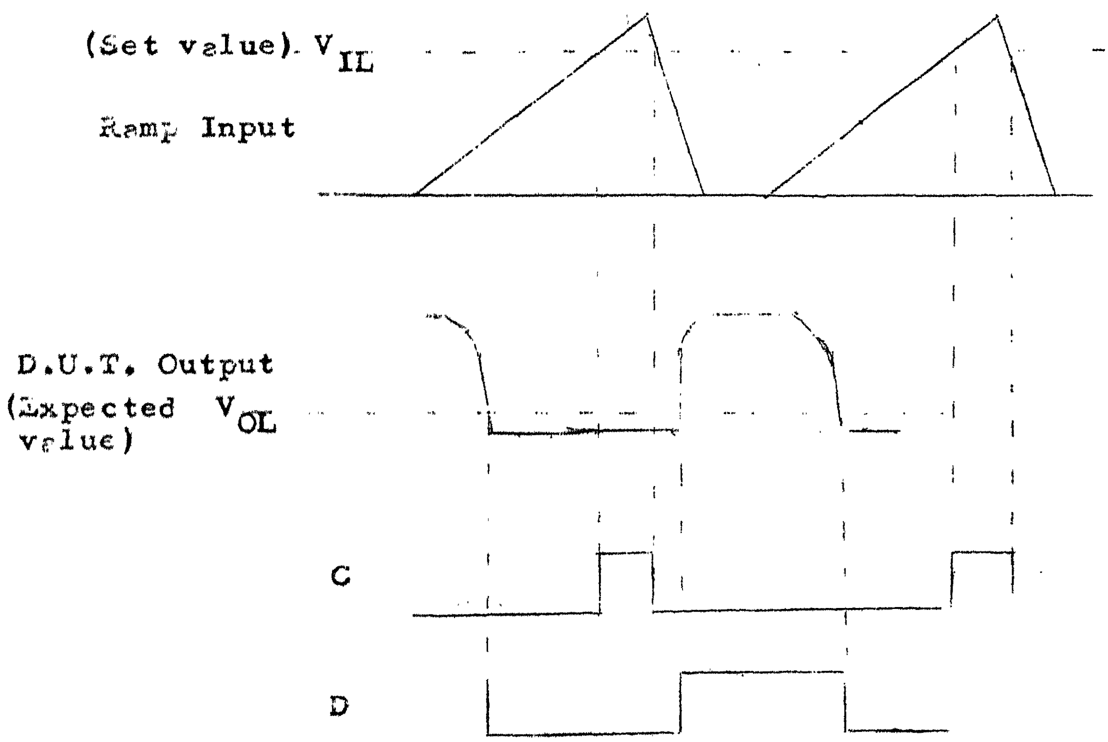



Fig. 5.2(b) $V_{OL}$ Test-waveforms

for a gate to pass this test is that both the outputs of the comparators should never be high at the same time. A NAND gate is used to detect the failure condition.

## 5.5 THRESHOLD TEST

Threshold is the simplest parameter to measure in a laboratory. It is measured simply by connecting output and input of the gate and measuring the input (output) voltage. It is usually specified by an upper limit and a lower limit. Hence a High-Low-Normal test is necessary in the case of threshold. It becomes complicated to do this test in an automatic scheme for the simple reason that the input and output of the gate are to be connected by a switch with negligible impedance which, as already pointed out in section 3.6, requires the use of reed relays. But since a complete test requires that the same test be repeated for all values of fan out, use of reed relays will obviously limit the test speed considerably.

The same swept-input method is therefore preferred here also and the output voltage of the D.U.T. is compared with the input by a comparator which changes state the moment these become equal. The ramp input is applied to a sample and hold circuit as shown in fig. 5.3(a), the sample and hold times being controlled by the output of the compartor. The amplitude of the sampled output pulse

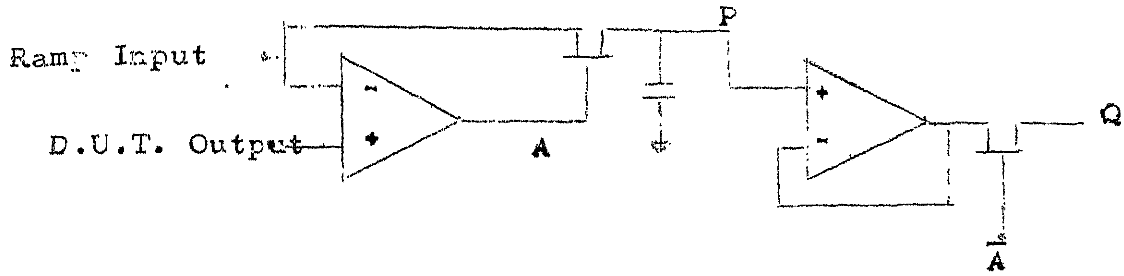



Fig. 5.1(a) Threshold Test Scheme

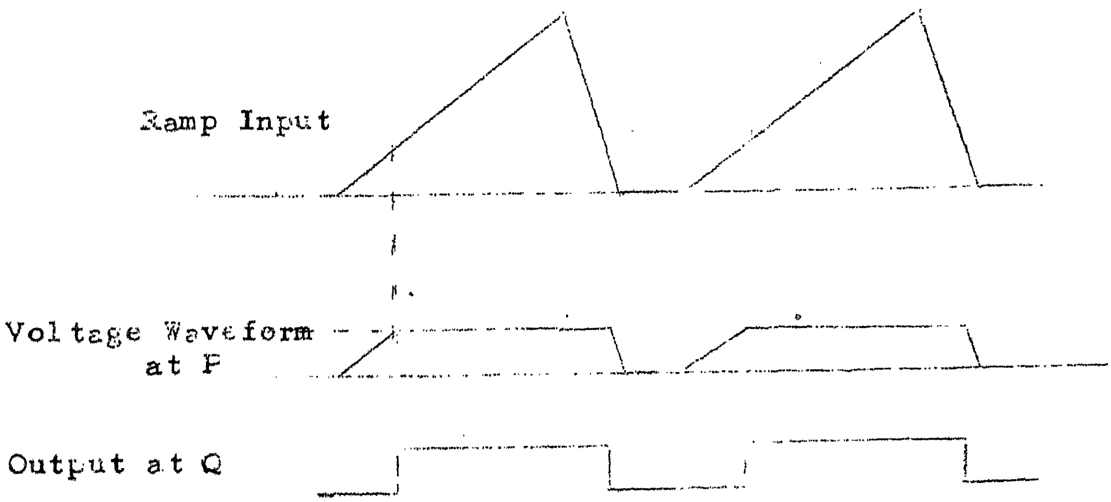
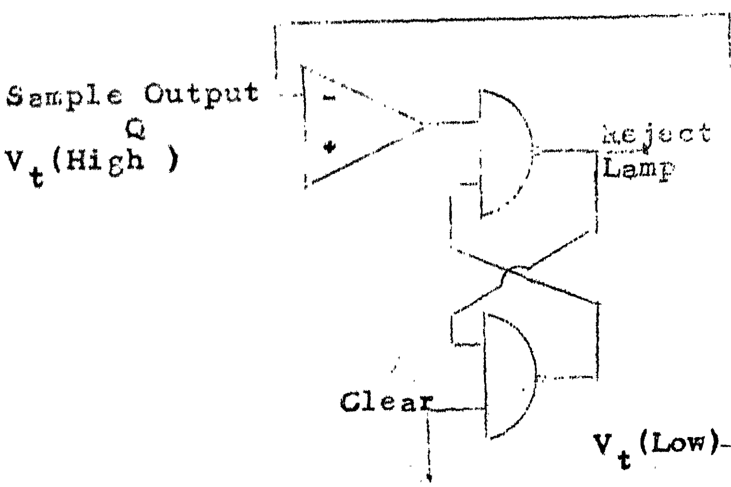



Fig. 5.1(b) Waveforms



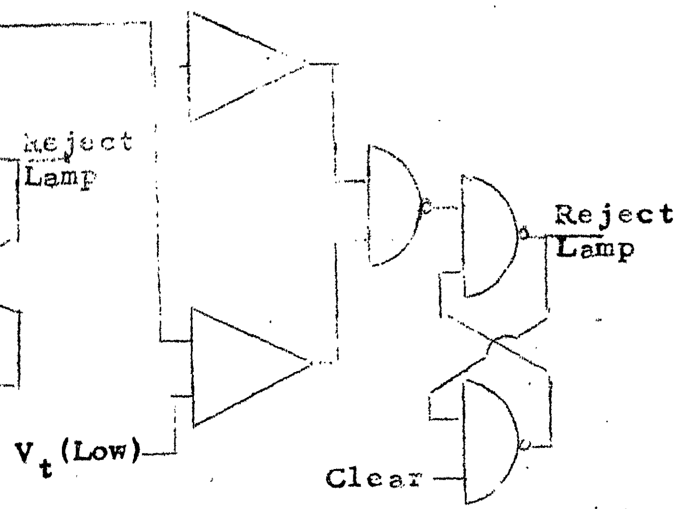




Fig. 5.1(c) $V_t$(High) Test    Fig.5.1(d) $V_t$(Low) Test

is equal to the threshold voltage $V_t$ . This value is compared against expected limits for a High- Low-Normal result. The output waveforms at various points are shown in Fig. 5.3(b). The sampled output pulse is compared with the upper acceptable limit of $V_t$ (Ref. Fig. 5.3(c)) and if the pulse amplitude is more than the upper limit, the comparator changes state. This information is stored in a latch to turn on a reject lamp, indicating that the measured value of $V_t$ is more than the acceptable upper limit. But, if the sampled output does not cross the lower limit, then this also is to be detected. For this, two comparators are necessary as shown in Fig. 5.3(d). The sampled output is fed to a zero crossing detector whose output is high during the hold time. The sampled output and the lower threshold limit are compared and the comparator output is low if the measured $V_t$ is more than the lower limit. Both output of the compartors in high states indicate that the measured $V_t$ is less than even the lower limit $V_t$ set. This condition is again detected by NANDing the outputs of the comparators.

## 5.6 UNITY GAIN POINT TESTS

The unity gain point $V_{UL}$ is usually specified by its minimum acceptable voltage limit while the unity gain point $V_{UH}$ is specified by its maximum acceptable

voltage limit. The procedure used in testing these parameters is to sweep the input voltage through its entire range and to check at the limits specified whether the unity gain points have already been reached or not. For a gate to pass the $V_{UL}$ test, the $V_{UL}$ point should not be reached earlier than the expected voltage setting of $V_{UL}$ when the input voltage is increasing.

Similarly for a gate to pass the $V_{UH}$ test, the $V_{UH}$ point should not be reached earlier than the expected voltage setting of $V_{UH}$ when the input voltage is reduced from $V_{CC}$.

It is clear from the transfer characteristic of a TTL inverter that as the input voltage is increased from zero the slope of the transfer characteristic increases from nearly zero and reaches unity when the unity gain point $V_{UL}$ is reached. Hence it is obvious that to obtain the slope information of the transfer characteristic, the output of the D.U.T. when the input is a ramp, requires to be differentiated.

### 5.6.1 <u>$V_{UL}$ Test</u>

The output of the D.U.T. when the input is a ramp voltage and its differentiated output are shown in Fig.5.4(a). It is clear from the figure that the unity gain point $V_{UL}$ corresponds to points P and R in the differentiated output. The ramp voltage input and the expected value of

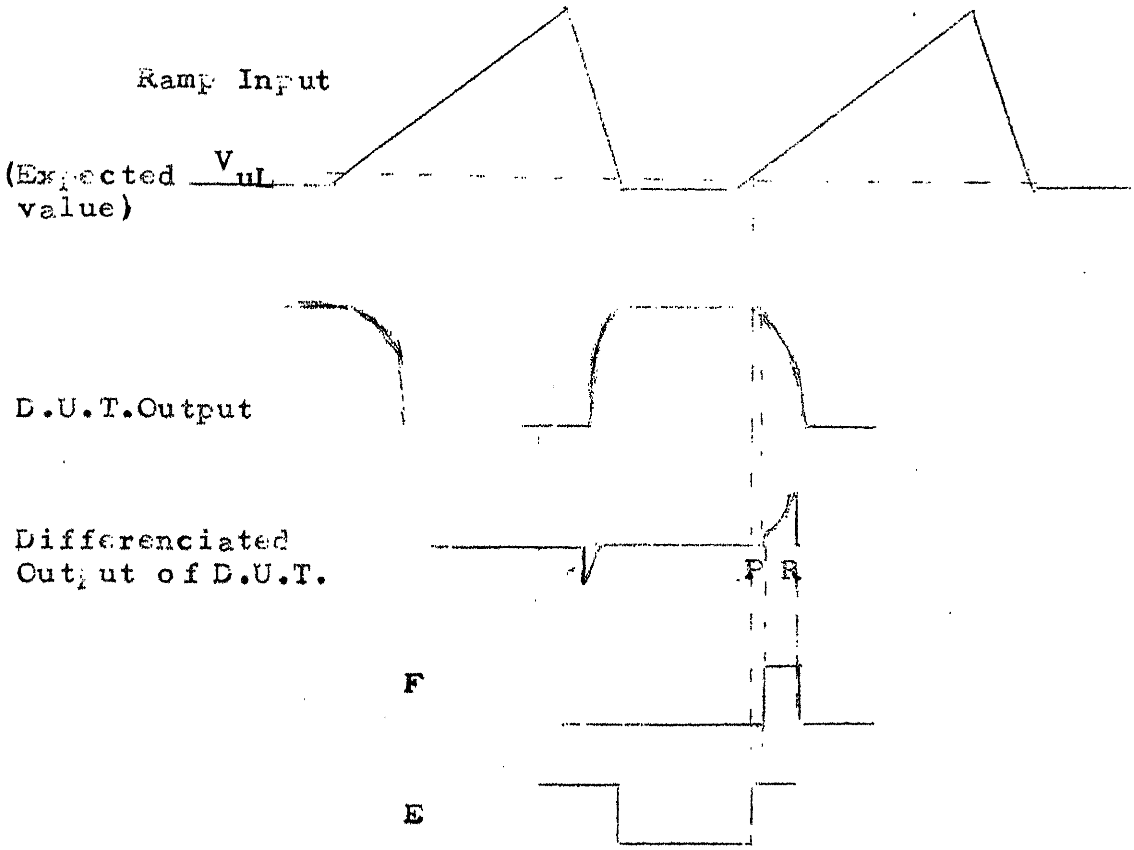



Fig. 5.4(a) $V_{uL}$ Test-waveforms

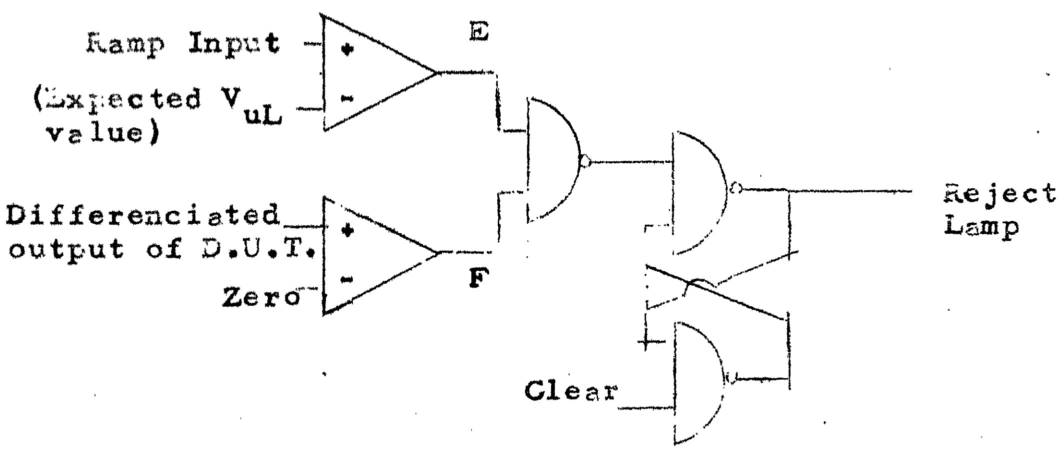



Fig. 5.4(b) $V_{uL}$ Test scheme

$V_{UL}$ are fed to a comparator whose output (E) is high if the ramp voltage is more than the expected value of $V_{UL}$. The differentiated output of the D.U.T. is fed to a zero crossing detector whose output (F) is high as long as the input is more than zero. The requirement for a gate to pass this test is that both the outputs E and F should never be high at the same time. This condition is detected by NANDing E and F.

### 5.6.2 $V_{UH}$ Test

It is clear from Fig. 5.5(b) that the unity gain point $V_{UH}$ corresponds to points Q and S in the differentiated waveform of the D.U.T. output voltage. Since it is much easier to detect the unity gain point $V_{UH}$ as the input voltage decreases from $V_{CC}$, this test is performed during the retrace of the ramp voltage. A gate pulse (G) is generated using a zero crossing detector which is high as long as the differentiated output is below zero. The ramp input and the expected value of $V_{UH}$ are fed to a comparator whose output (H) is high when the ramp voltage is more than the expected value of $V_{UH}$ Ref. Fig. 5.5(a). For a gate to pass this test, both the outputs G & H should never be high at the same time, which is detected by NANDing G and H outputs. The waveforms are given in Fig. 5.5(b).

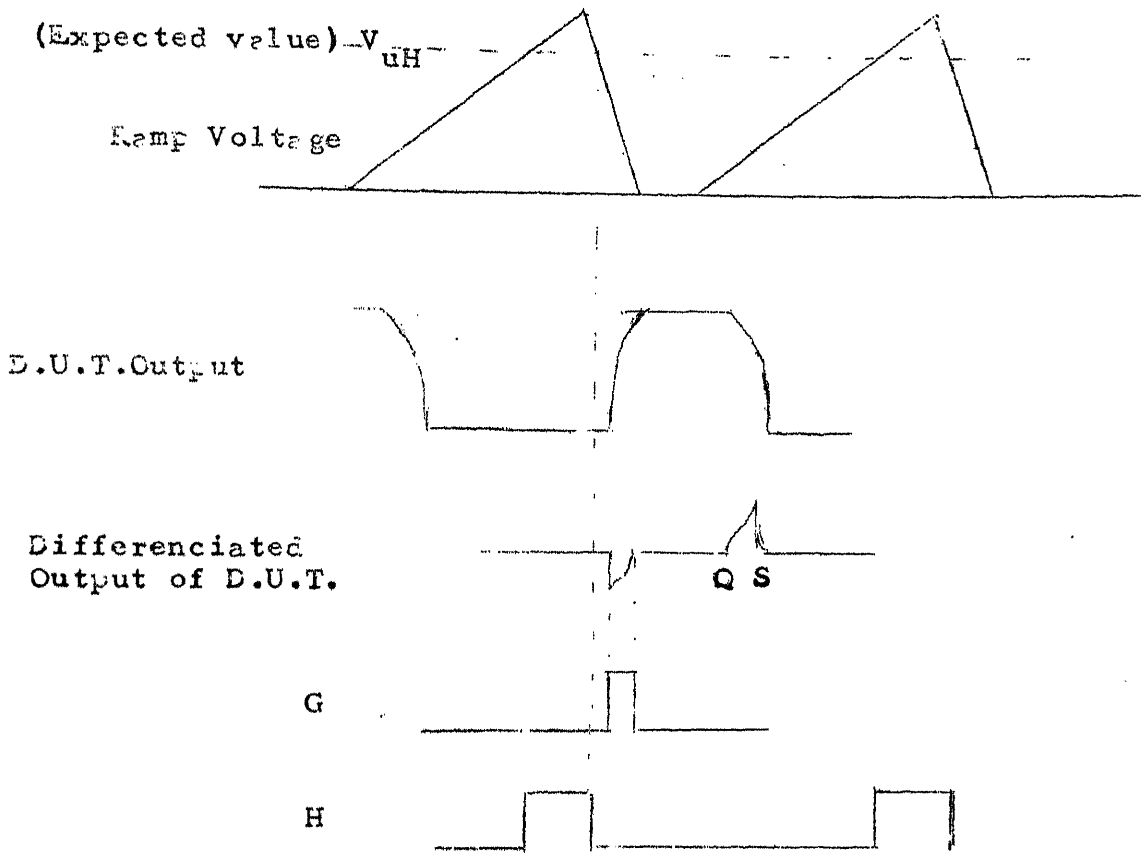



Fig. 5.5(a) $V_{uH}$ Test-waveforms

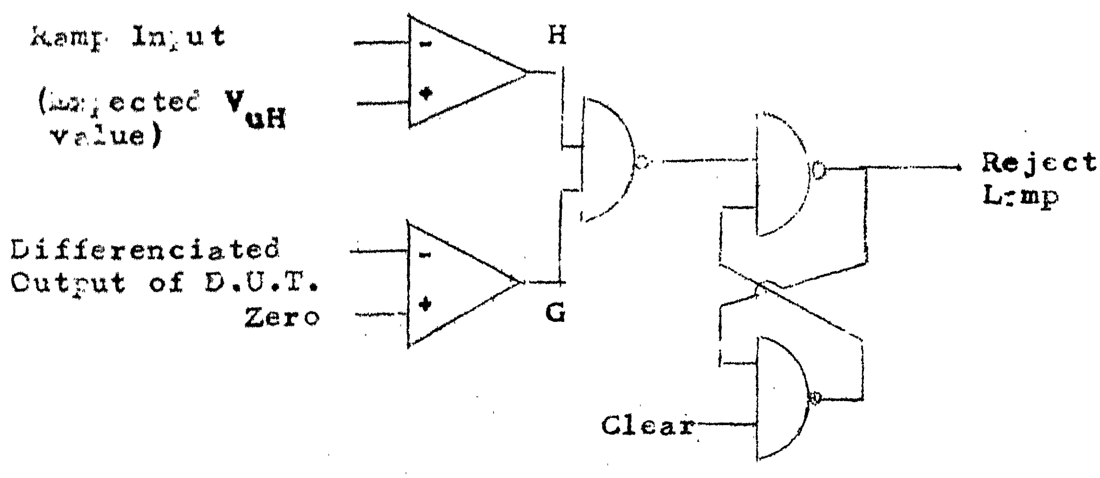



Fig. 5.5(b) $V_{uH}$ Test scheme

## 5.7 INPUT CURRENT TESTS

Input current measurement on a device normally poses a problem since this measurement is to be made without affecting the operation of the device.

The circuit which can be used for measuring $I_{iL}$ and $I_{iH}$ of a gate is shown in Fig. 5.6. The fact that for an operational amplifier working in the linear range, the voltage difference between the non-inverting and inverting inputs is ideally zero is made use of here. The D.U.T. input is connected to the emitter of the transistor. The input voltage applied to non-inverting input appears exactly at the input of the D.U.T., while an independent terminal (collector of transistor) is available for making measurements When there is no input current from or into the device,

$$V_{O1} = V_{CC} - I_o R \qquad (V.1)$$

when the input current from the device is I

$$V_{O2} = V_{CC} - (I_o - I)R \qquad (V.2)$$

Hence the difference voltage $V_{01} - V_{02} = IR$ is a measure of the input current I. The same set up can be used for both $I_{iL}$ and $I_{iH}$ measurements.

Since the collector of the transistor has a quiescent voltage, in order to make automatic measurements simpler, other identical circuit described above

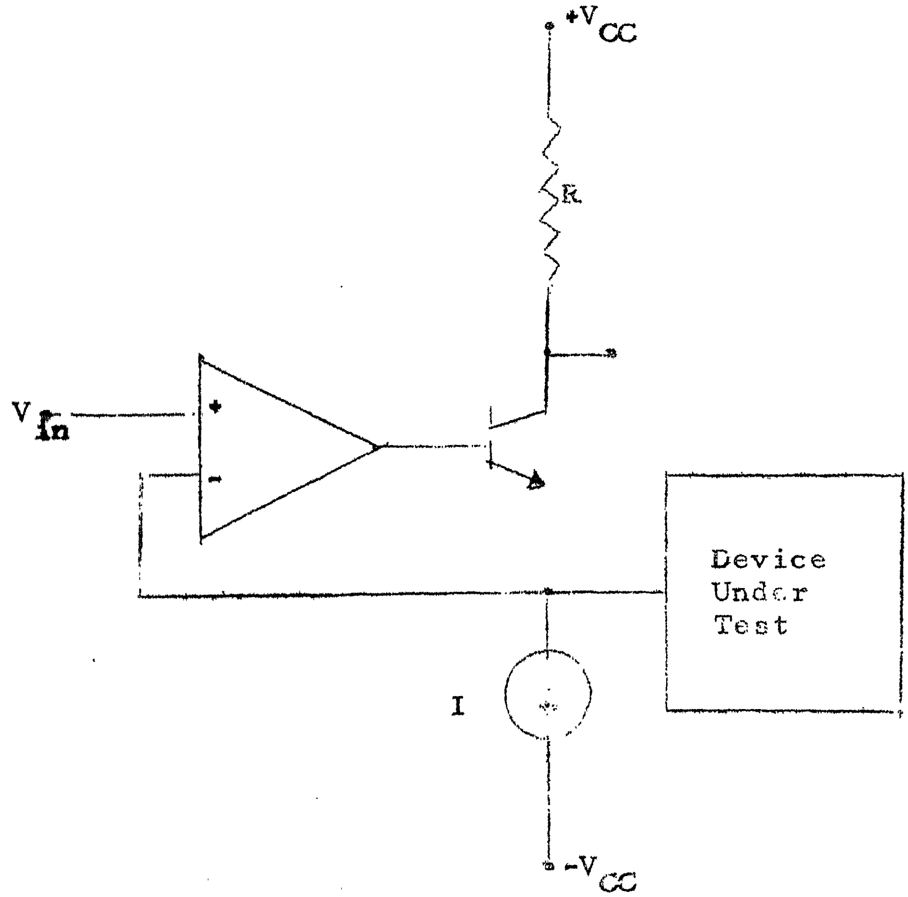



Fig. 5.6 Input Current Tests

is made use of. But the D.U.T. input is connected to emitter of one unit only and the voltage difference between the collector terminals is fed to a difference amplifier to get a single ended output proportional to I. This can be compared with expected currents for a GO/NO-GO result.

## 5.8 POWER SUPPLY CURRENT TESTS

Power supply current is another important parameter to be measured in IC testing and is usually specified by maximum currents $I_{CCL}$ and $I_{CCH}$ under both logical conditions of output. Resistor values are difficult to control exactly in IC manufacturing and if resistors are too low in value, resulting high current could cause power supply and heating problems. The supply current $I_{CC}$ is measured under both logical conditions using a scheme similar to input current test scheme discussed in the previous section. Instead of the D.U.T. input the power supply terminal of the D.U.T. is connected to the emitter of the transistor (Ref Fig. 5.7). The exact power supply voltage is applied to the non-inverting input of the operational amplifier. The voltage proportional to the power supply current is obtained as before and this can be compared against limits to produce a GO / NO-GO result.

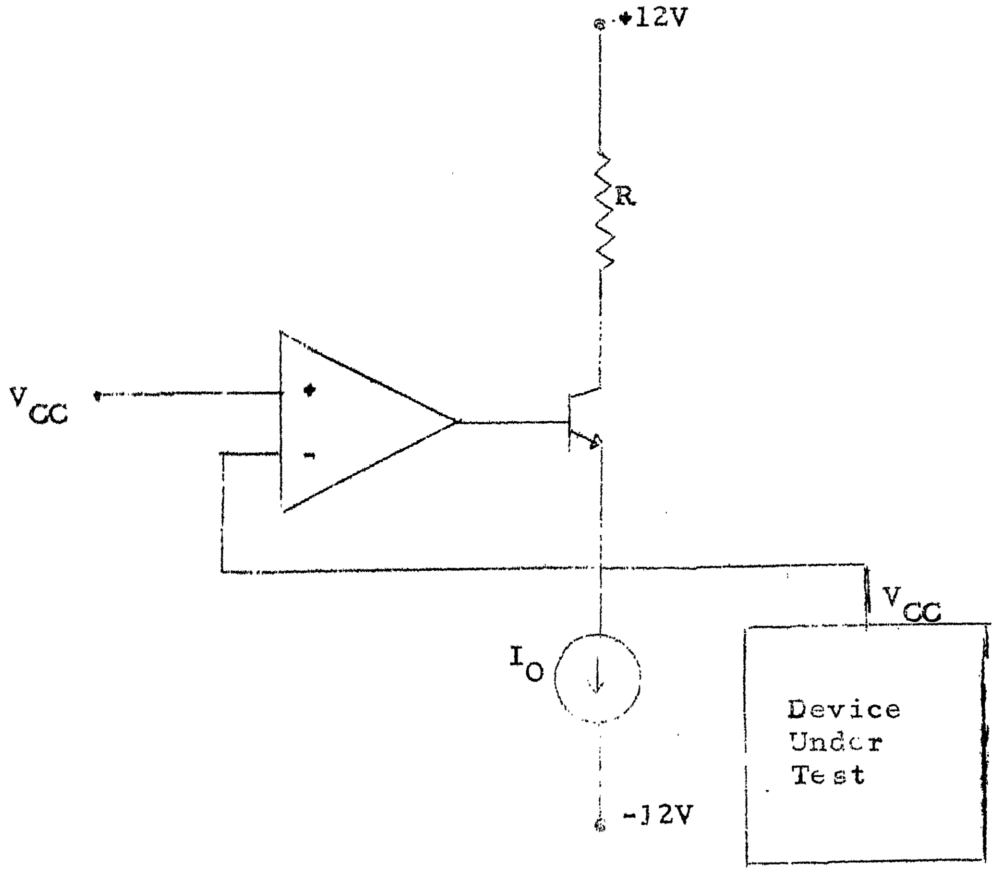



Fig. 5.7 Power Supply Currents Test

# CHAPTER VI

## PARAMETRIC TESTER DESIGN

The principle of automatic parametric testing has been discussed in the previous chapter. The advantages of the swept-input testing, forced current loading of D.U.T. autputs and the necessity for a threefold sequencing for testing any multiple, multi-input NAND/NOR gate chip has been pointed out. Based on these considerations the system design of a GO/NO-GO type of parametric tester is discussed in this chapter. The programming necessary for the automation has been done using plug-in printed cards. A coding scheme similar to that used in the design of the Functional Tester has been used.

### 6.1 SYSTEM DESCRIPTION

A simplified block diagram of the parametric test unit is shown in Fig. 6.1. The instrument consists of the following main blocks.

1. Gated Astable and Ramp Generator
2. Fan out Counter
3. Input Counter
4. Gate Counter
5. Input Selector

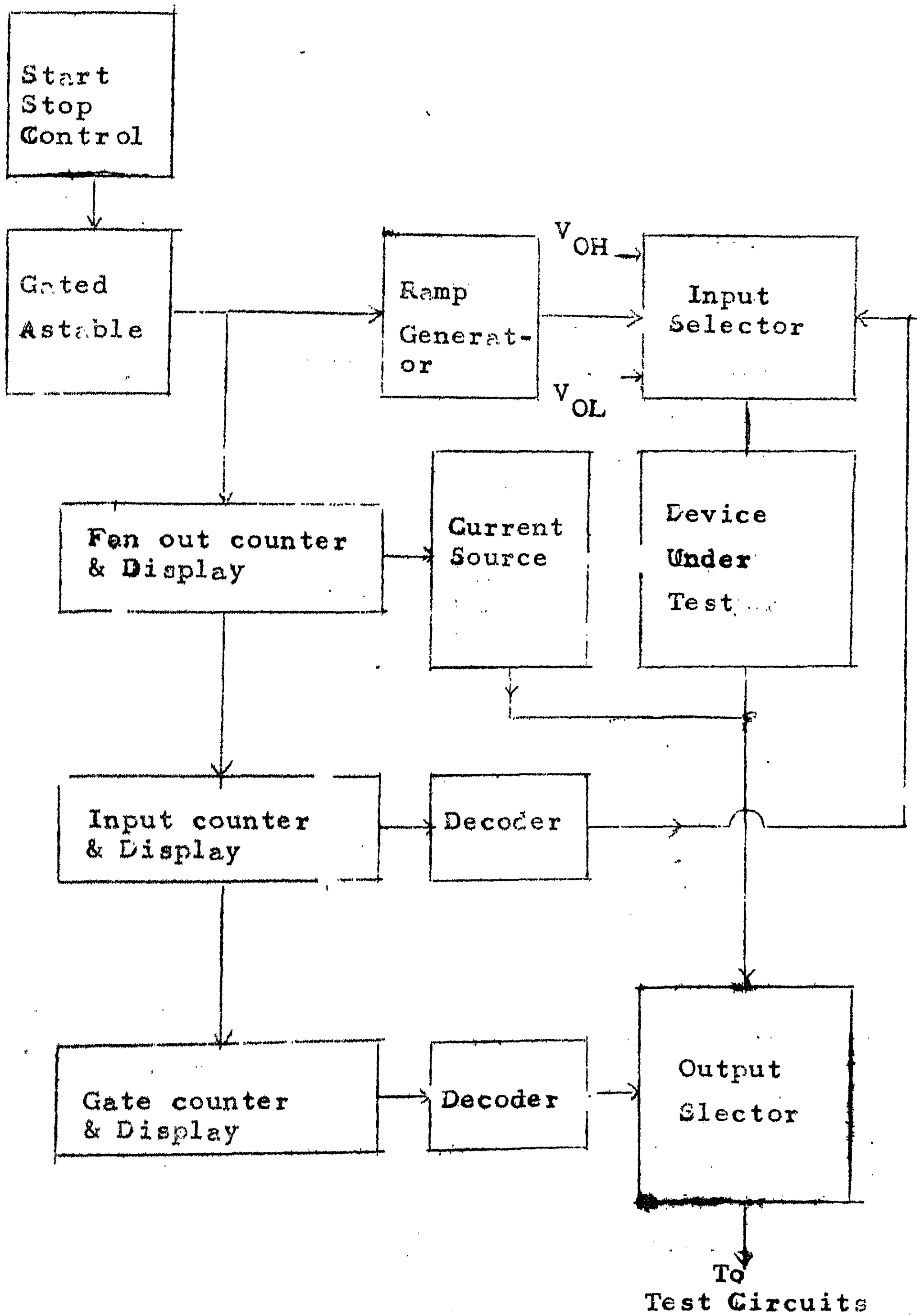



Fig.6.1 Block diagram of the Parametric Tester

6. Output Selector

7. Comparators

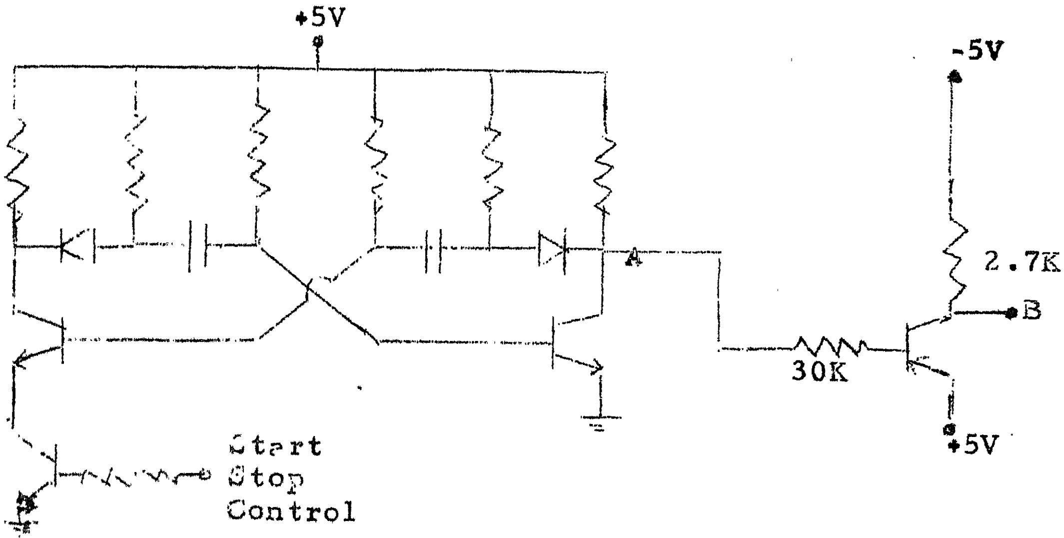
8. Current Source

The functions of these blocks and the considerations involved in their design are briefly pointed out in the following sections.

## 6.2 GATED ASTABLE AND RAMP GENERATOR

It is desired that on the application of a 'start' signal, the testing should be started and as soon as a failure is detected the testing should be stopped. After the failure is taken note of, it may be necessary in the case of multiple gates to continue the tests from the next gate of the same chip. Hence a ramp voltage generator controlled by a gated astable multivibrator is made use of.

The circuit diagrams of the Gated Astable and the Ramp Generator are given in Fig. 6.2(a). The rectangular waveform output from the astable multivibrator controls the current switch consisting of four diodes $D_1, D_2, D_3, D_4$ and the resistors $R_1, R_2$. Thus the direction of current flow through the capacitor C is controlled to get a ramp voltage waveform. A diode across the capacitor in the feed back path of the operational amplifier, prevents the ramp voltage from going to negative values more than a diode drop.



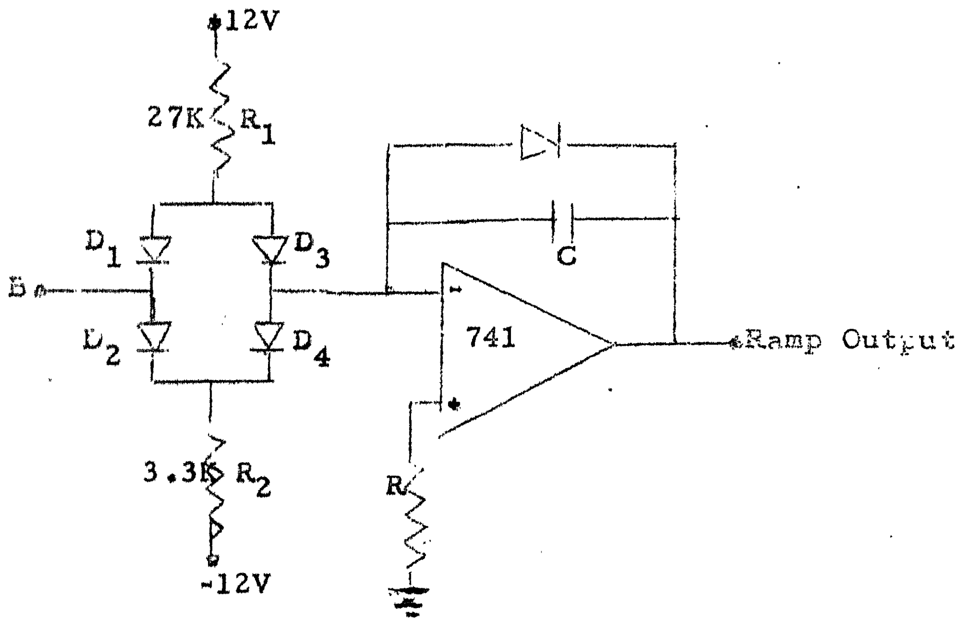




Fig.6.2(a) Gated Astable and Ramp Generator

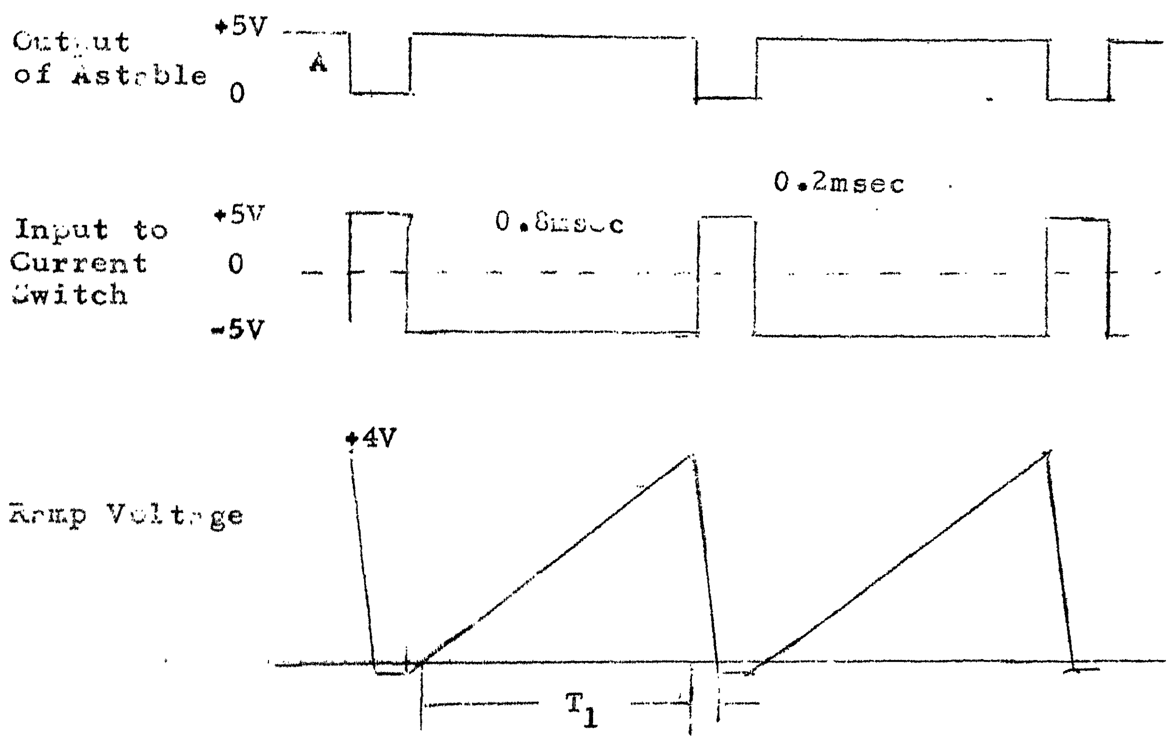



Fig. 6.2(b) Gated Astable and Ramp Generator Output Waveforms

When the output of the astable is nearly 5 Volts the transistor $T_3$ is off and diodes $D_1$ & $D_4$ conduct and current through $R_2$, $D_4$ and C causes the output voltage to increase. When the output of the astable(A) is nearly zero ($V_{CE\ sat}$) then transistor $T_3$ is also in saturation and the diodes $D_2$ & $D_3$ conduct while $D_1$ & $D_4$ are OFF. Thus current flows through C $D_3$ and $R_1$ and the ramp voltage decreases.

The period of the astable is chosen to be 1KHz, considering the speed and hardware limitations, especially the speed of comparators which are necessary for the testing and measurements.

The maximum voltage reached by the ramp is limited to about 4 Volts and with a chosen value of 0.1 $\mu$F for C, the values of $R_1$ and $R_2$ are calculated from the relations

$$(V + V_d) = \frac{1}{C} \left( \frac{V_{CC} - V_d}{R_2} \right) T_1 \qquad \text{(VI.1)}$$

$$(V + V_d) = \frac{1}{C} \left( \frac{V_{CC} - V_d}{R_1} \right) T_2 \qquad \text{(VI.2)}$$

with $T_1$ = 0.8 msecond and $T_2$ = 0.1 msecond the values of $R_1$ and $R_2$ are nearly 27K$\Omega$ and 3.3K$\Omega$. The waveforms of the output of the astable and the ramp generator are shown in Fig. 6.2(b).

The output of the Gated Astable is fed to a PNP transistor switch, as shown, to get a rectangular waveform which has both positive and negative excursions, necessary to control the current switch.

## 6.3 FAN OUT COUNTER

Since it is essential to conduct parametric tests under all fan out conditions up to the maximum specified for the device, a 6-bit synchronous BCD counter, which indicates the fan out at any time, is made use of. Since the maximum fan out limit specified is 30 for TTL Buffer gates (F=0) and 10 for other TTL gates ( F = 1), this counter must count upto a maximum of 10 or 30 depending upon the device, as specified by the code in the programmed circuit card.

The clock for this synchronous counter is from the Gated Astable. The output of this counter is fed as clock to the Input Counter. The logical expressions for the various inputs of the flip-flops constituting this counter are given below.

$$J_{F1} = \bar{Q}_{F5} + \bar{F} \; \bar{Q}_{F6} = K_{F1}$$

$$J_{F2} = Q_{F1} \; \bar{Q}_{F4} = K_{F2}$$

$$J_{F3} = Q_{F1} \; Q_{F2} = K_{F3}$$

$$J_{F4} = J_{F3} \; Q_{F3}$$

$$K_{F4} = Q_{F1} \; Q_{F4}$$

$$J_{F5} = \overline{J_{F1}} + K_{F4} = K_{F5}$$

$$J_{F6} = \overline{F}\cdot K_{F4} + Q_{F5}$$

$$K_{F6} = Q_{F5}\cdot Q_{F6}$$

where $Q_{F1}$, $Q_{F2}$, ------ $Q_{F6}$ are the outputs of the six flip-flops of this counter.

## 6.4 INPUT COUNTER

This 3-bit synchronous counter is necessary to contain the input number of the gate being tested. The clock of this counter is $O_F$, the output of the fan out counter. But if the device is an inverter, this counter is not incremented at all. The maximum count reached by this counter depends on the number of inputs to the gate under test and is decided by the codes D and E in the programme programmed circuit card.

The logical expressions for the various inputs of the three flip-flops of this counter are given by

$$J_{I1} = \overline{\overline{D}\cdot E\cdot Q_{I2}} = K_{I1}$$

$$J_{I2} = \overline{D}\cdot\overline{E}\cdot Q_{I1} + J_{I1} = K_{I2}$$

$$J_{I3} = D\cdot E\cdot Q_{I1}\cdot Q_{I2} = K_{I3}$$

$$\text{Clock} = \overline{A}\cdot O_F$$

where $Q_{I1}$, $Q_{I2}$, $Q_{I3}$ are the outputs of the three flip-flops of this counter and $O_F$ is the output of the fan out counter.

The expressions for the outputs of this counter are

$$Y_I = \bar{D}.E.Q_{I2} + \bar{E}.Q_{I1}.(\bar{D} + Q_{I2}) \quad \text{and}$$

$$Z_I = D.E.\ Q_{I1}.Q_{I2}.Q_{I3}$$

where the output $Y_I$ is used for incrementing the Gate Counter while $Z_I$ is the TEST OVER signal in case the gate under test is an 8-input gate and therefore has a single output. The Gate Counter is not incremented in this case.

## 6.5 GATE COUNTER

This 3-bit synchronous counter is necessary to contain the gate count. Since the number of inputs of a gate also determines the number of such gates in that chip, the codes D and E are used here also in determining the maximum count reached by this counter. Once the maximum gate count for the device is reached, a TEST OVER signal is generated. The logical expressions for the inputs of the flip-flops of this counter are given by

$$J_{G1} = A + \bar{E} + \bar{D}.Q_{G2} = K_{G1}$$

$$J_{G2} = A.\bar{Q}_{G1}.\bar{Q}_{G3} + \bar{A}.\bar{D}(Q_{G1} + E.Q_{G2})$$

$$J_{G3} = A.Q_{G1}\ (Q_{G2} + Q_{G3})$$

where $Q_{G1}$, $Q_{G2}$, $Q_{G3}$ are the outputs of the three flip-flops of this counter. The clock of this counter is $O_F$ the output of the Fan out Counter, if the D.U.T. in an

inverter;otherwise $Y_1$ the output of Input Counter in the case of a multi-input gate.

## 6.6 INPUT SELECTIOR

As pointed out in the previous Chapter, all the parametric tests are to be done on each of the inputs of the D.U.T, one at a time, while the other inputs are disabled. It is therefore, necessary to hold the other inputs of the gate at appropriate logic states, usually at the worst case limits for these states. For NAND gate this level is clearly $V_{IH}$ and for NOR it is $V_{IL}$. The function of the Input Selector is to select the appropriate input of the gate to be tested and to apply appropriate voltages (ramp voltage, $V_{IL}$ or $V_{IH}$) to all the inputs of the gate. A decoder selects the input to be tested according to the contents of the Input Counter. The selection of appropriate voltages to be applied to the inputs of the D.U.T. is done using FET switches as shown in Fig. 6.3(a). An operational amplifier as source follower is used after the switches. It is not desirable to allow gate input current to pass through these FET switches, which may have considerable ON resistance. Hence an operational amplifier is necessary after these switches to take care of the sourcing or sinking current at the gate input. The logical expressions to control the three FET switches are given by

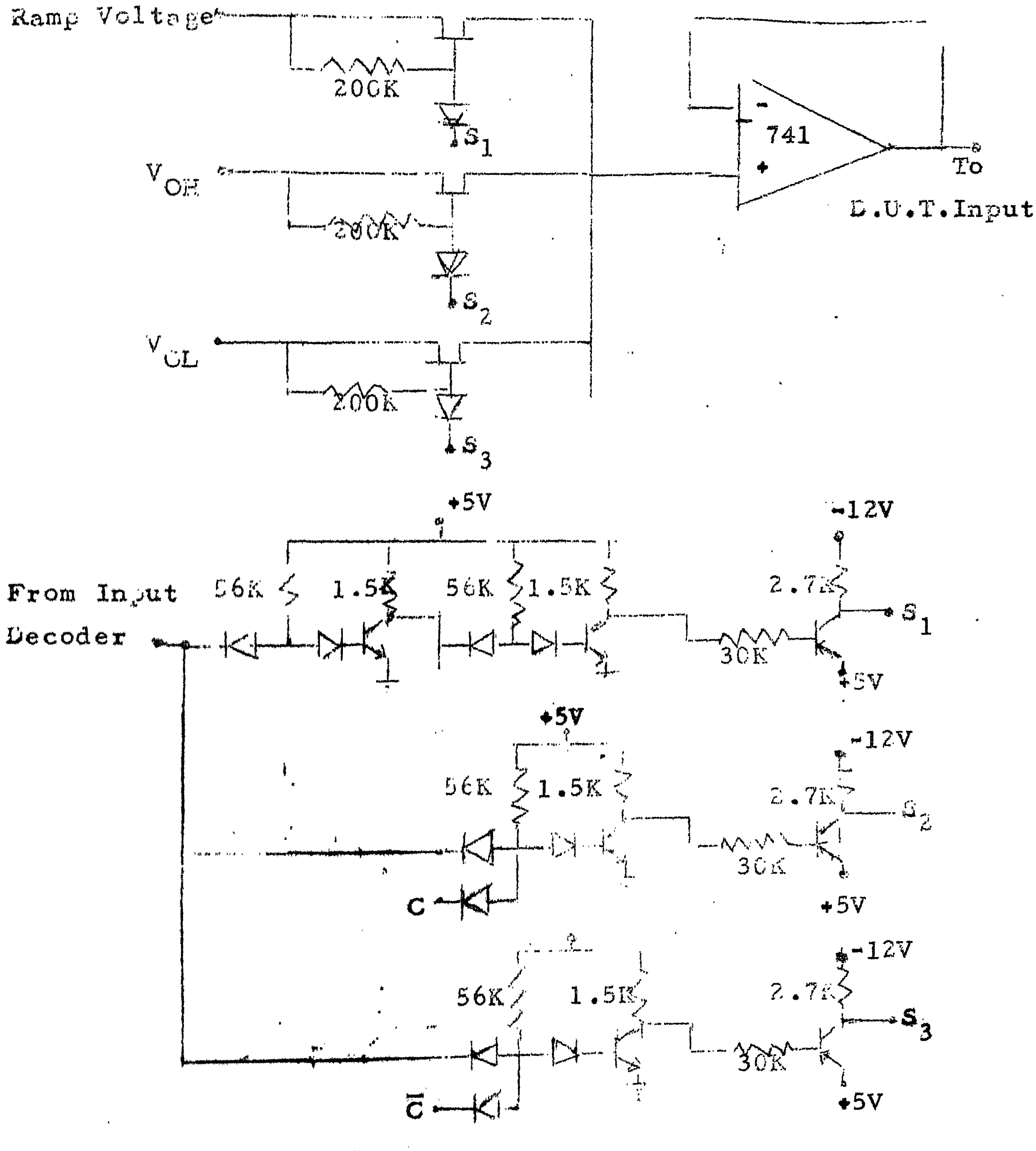



Fig. 6.3.Input Selector

$S_1 = ID$

$S_2 = \overline{ID}.C$

$S_3 = \overline{ID}.\overline{C}$

where ID is the appropriate selected input as found from the decoder associated with the Input Counter.

The logic levels of +5 volts and -12 volts for $S_1, S_2$ $S_3$ are necessary to completely switch the FET either ON or OFF. The realizations of these logical expressions are shown in Fig. 6.3(b).

Eight units similar to the one shown here is necessary so that any gate which has upto 8 inputs can be tested.

## 6.7 OUTPUT SELECTOR

The requirement that all the gates of the D.U.T. are to be tested sequentially, indicates the need for selecting the appropriate output for measurement purposes. FET swtiches followed by operational amplifier in source follower configuration is used as the Output Selector (Fig. 6.4). Six switches are necessary since there can be at most six outputs from the devices we have selected for testing. The low impedance of the operational amplifier which follows the FET switches takes care of the loading, if any, of the measurement circuits.

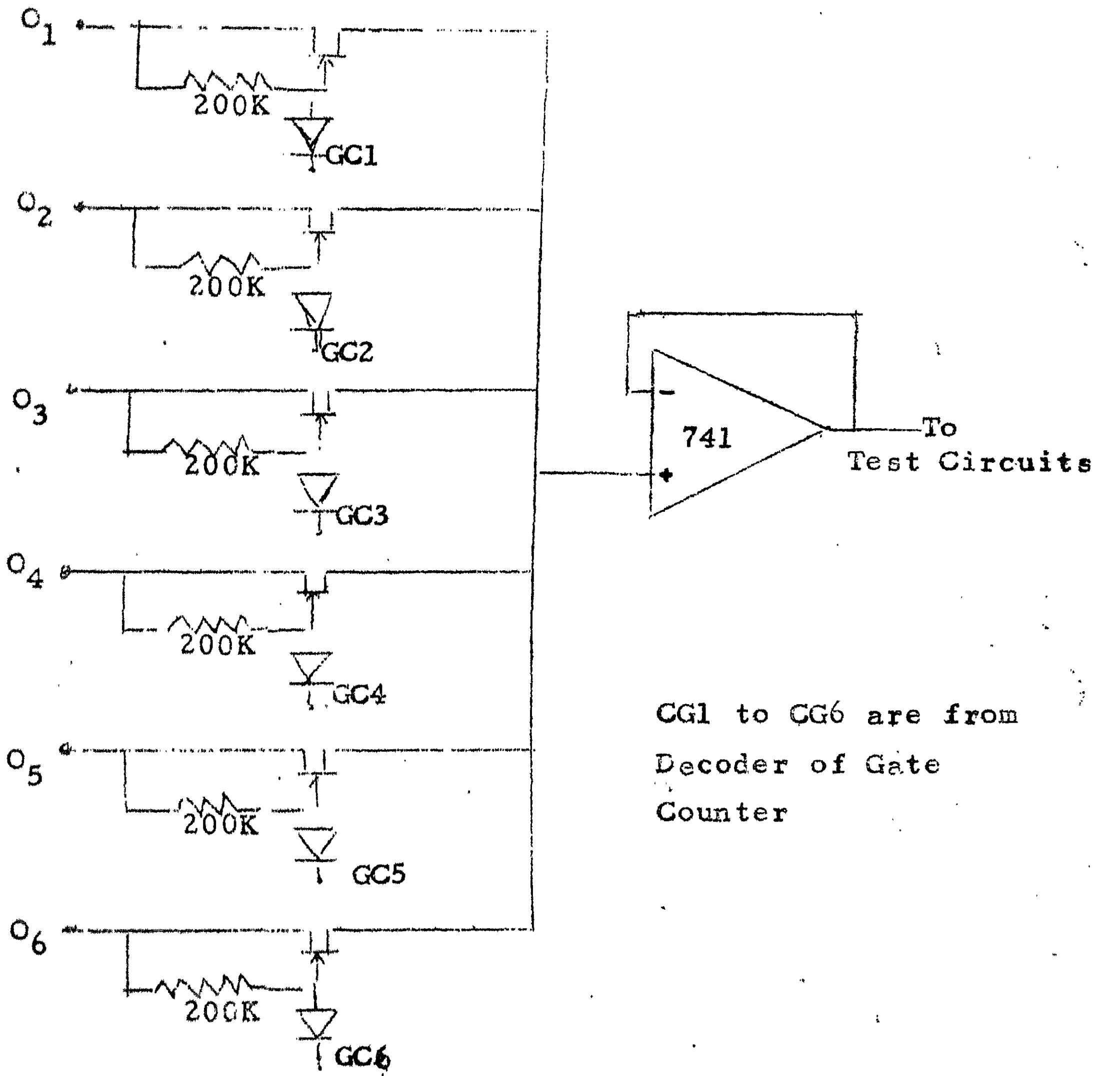



Fig.6.4.Output Selector

## 6.8 COMPARATOR

The comparator is an important circuit block in this instrument, for the accuracy of measurements of many parameters depends on what is called the 'dead zone' of the comparator. The dead zone indicates the magnitude of the minimum difference input that must be applied to the comparator before it changes state. The frequency response of the comparator is another important parameter on which the testing speed depends.

Operational amplifiers (ECO 709), operated with supply voltages + 5 and - 5 Volts are used as comparators in this instrument. The open-loop gain of this amplifier is around 5000, when operated with ± 5 Volts power supplies and it is found that there is no problem of oscillations, when the amplifier is operated in the open-loop configuration as a comparator.

## 6.9 CURRENT SOURCE

The advantages of forced current loading have been explained in section 5.3. A current whose magnitude is proportional to the fan-out count is to be either forced into the D.U.T. output or removed from it. Hence a bi-directional current source is necessary for this puppose. A simple method to generate current whose magnitude is proportional to the fan-out count is to obtain a a voltage which is proportional to the fan out count and

use this voltage as input to a Voltage Controlled Current Source (VCCS).

Using a set of weighted resistances and a summing amplifier as shown in Fig. 6.5, a voltage proportional to the fan out count is obtained. In order that the voltages that are applied to the input resistances of the summing amplifier are very nearly GND and 5 volts, transistor switches are used in inverted mode of operation. Since the Fan out Counter is a BCD counter the resistances at the input of the summing amplifier are to be chosen as R, R/2, R/4, R/8, R/10 and R/20. By choosing R=300K and $R_2$ = 10K the maximum output voltage of the summing amplifier is obtained to be around 5 volts.

A simple bi-directional current source is shown in Fig. 6.6(a). For an operational amplifier working in the linear range the voltage difference between non-inverting and inverting inputs is ideally zero and hence the input voltage applied to the non-inverting amplifier appears exactly at the emitter of the transistor. Hence

$$I_2 = \frac{V_{in} - (-V_{CC})}{R} = \frac{V_{in} + V_{CC}}{R}$$

Another simple current source $I_1$ is connected to the collector of the transistor as shown. The difference current $I_1 - I_2$ flows into the load.

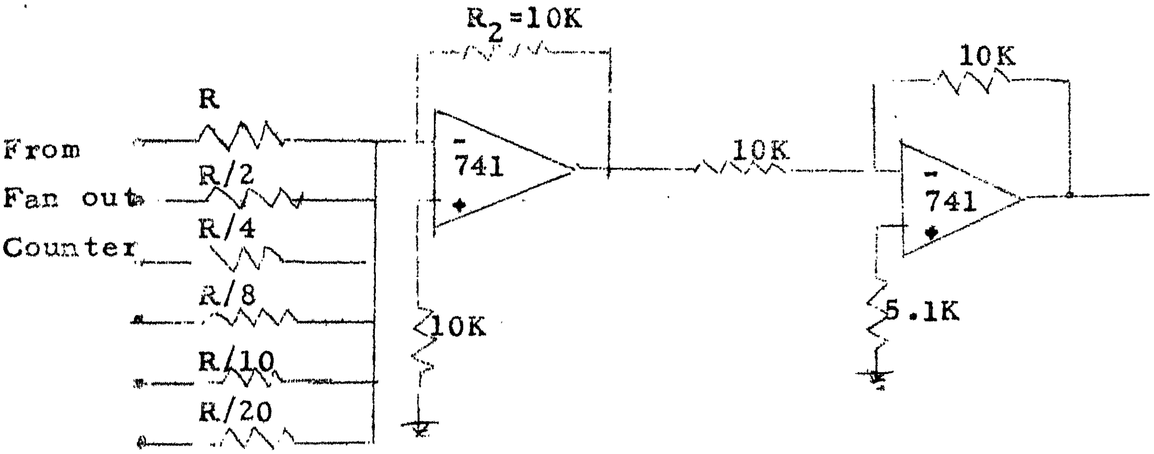



Fig. 6.5.D/A Converter

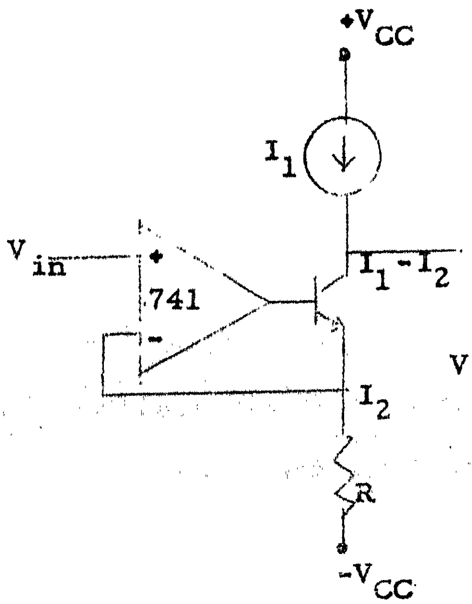



Fig. 6.6(a) Simple VCCS

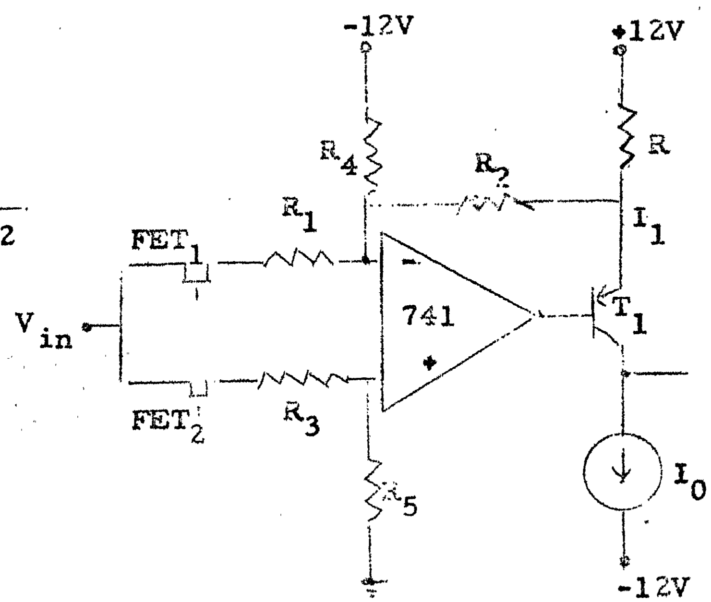



Fig. 6.6(b).A bi-directional VCCS

In order to get a bi-directional VCCS whose current magnitudes are controlled by a single voltage, the **circuit** as shown in Fig. 6.6(b) is used. The input is applied either to the non-inverting the inverting input of the operational amplifier, using two FET switches. When the current source is required to source current FET 1 is ON while the other FET is OFF and as input voltage increases, the emitter voltage of the transistor $T_1$ decreases and hence $I_1$ increases. Since $I_O$ is constant the difference current $I_1 - I_O$ that flows into the load increases. When the current source is required to sink current FET 2 is ON while FET 1 is OFF. An increasing input voltage causes emitter voltage of $T_1$ to rise, decreasing $I_1$. Hence a current of magnitude $I_O - I_1$ is removed from the load. $R_2$ and $R_4$ essentially bias the emitter voltage so that even with maximum input voltage there is sufficient voltage drop across the collector and emitter of the transistor $T_1$.

# CHAPTER-VII

# CONCLUSIONS

## 7.1 STATE OF HARDWARE BUILT AND COST

The Functional Tester has been entirely fabricated using indigenously available integrated circuits. Its working is found to be completely satisfactory. All the NAND/NOR gates of the 7400 series of TTL family and the three flip-flops,viz-SN 7473, SN 7474, SN 7470 can be tested reliably by this unit. Printed Circuit cards for most of the gates and flip-flops have been made. When circuit cards are not available for any device the patch board can be used to program in any desired manner. The parametric test unit could not be completed due to lack of time. Many of the blocks of this unit have been made and tested separately. The cost of the components alone in the Functional Tester unit is about Rs. 1000/- based on the present cost of IC's, while for the parametric test unit whose system design has been given in chapter VI this may be expected to be around Rs. 3000/-.

## 7.2 LIMITATIONS ON SPEED AND ACCURACY

In the Functional Tester unit which mainly consists of digital integrated circuits, speed is the most relevent factor apart from the reliability of the whole system. All the devices listed above have been tested to ensure

ensures that all transitions of the flip-flop are tested. The hardware requirements for this scheme for two specific types of flip-flops SN 7473 and SN 7474 are also given.

In the hardware programming scheme used in the project, the corresponding inputs of a multiple gate chip are brought out to same input terminals of the 22 pin connector. This makes measurement of certain parameters like input currents meaningless, since all corresponding inputs are always connected in parallel. Another possibility is to bring out all inputs of the device separately But the hardware requirement for the input selection unit using this scheme is quite large.

The magnitude and direction of current from the current source which leads the D.U.T. output is to be changed at the appropriate time to ensure the safety of the device. In the present case the device is loaded by currents corresponding to either logical 0 or logical 1 only and a better scheme would be to simulate the input current-input voltage characteristics and use this to apply currents of appropriate magnitude under all states of the device including the states between the extreme states.

In the testing of SN 7470 flip-flop, the asynchronous inputs are not tested at all in the present scheme. The asynchronous inputs in this case are effective only when the clock is low. Hence the scheme in which the initial

reliable operation of all circuit blocks of the system.

In parametric testing, all the test circuits involve the use of a large number of comparators. The frequency response and dead zone of the comparator place a limitations on the speed and accuracy of measurements. However as pointed out earlier, speed is rarely a criterion in such testers where devices are to be removed and inserted manually for testing.

Another possible source of error can be due to the finite ON resistances of FET switches. The input voltage applied to the D.U.T. is from the input selector unit while the ramp voltage used as input to various comparators is the output of the Ramp Generator. Any shift in the d.c. level of the ramp voltage as it passes through the switches can result in error in the measured values. This possibility is greatly reduced in our scheme by the use of an operational amplifier as a source follower, after the FET switches to ensure that no current passes through the FET switches.

## 7.3 POSSIBLE IMPROVEMENTS

The Testing scheme used for flip-flops, though satisfactory in most cases, is not exhaustive. Another possibility, in which the initial state of the flip-flop is brought to either 0 or 1 before the applications of each clock pulse is described in Appendix IV. This scheme

state is brought out to either 0 or 1, before the application of clock pulse can be used for a complete testing of this flip-flop.

# APPENDIX-I

The detailed circuit diagrams for all the blocks of the Functional Tester are shown in Figs. A-I.1 to A-I.11. The pin descriptions for each of the 22 pins of these cards are given in TABLES A-I.1 to A-I.11. In all the 11 cards used in the Functional Tester unit, pin No. 1 is used for GND while pin No. 22 is used for +5V power supply.

CARD A

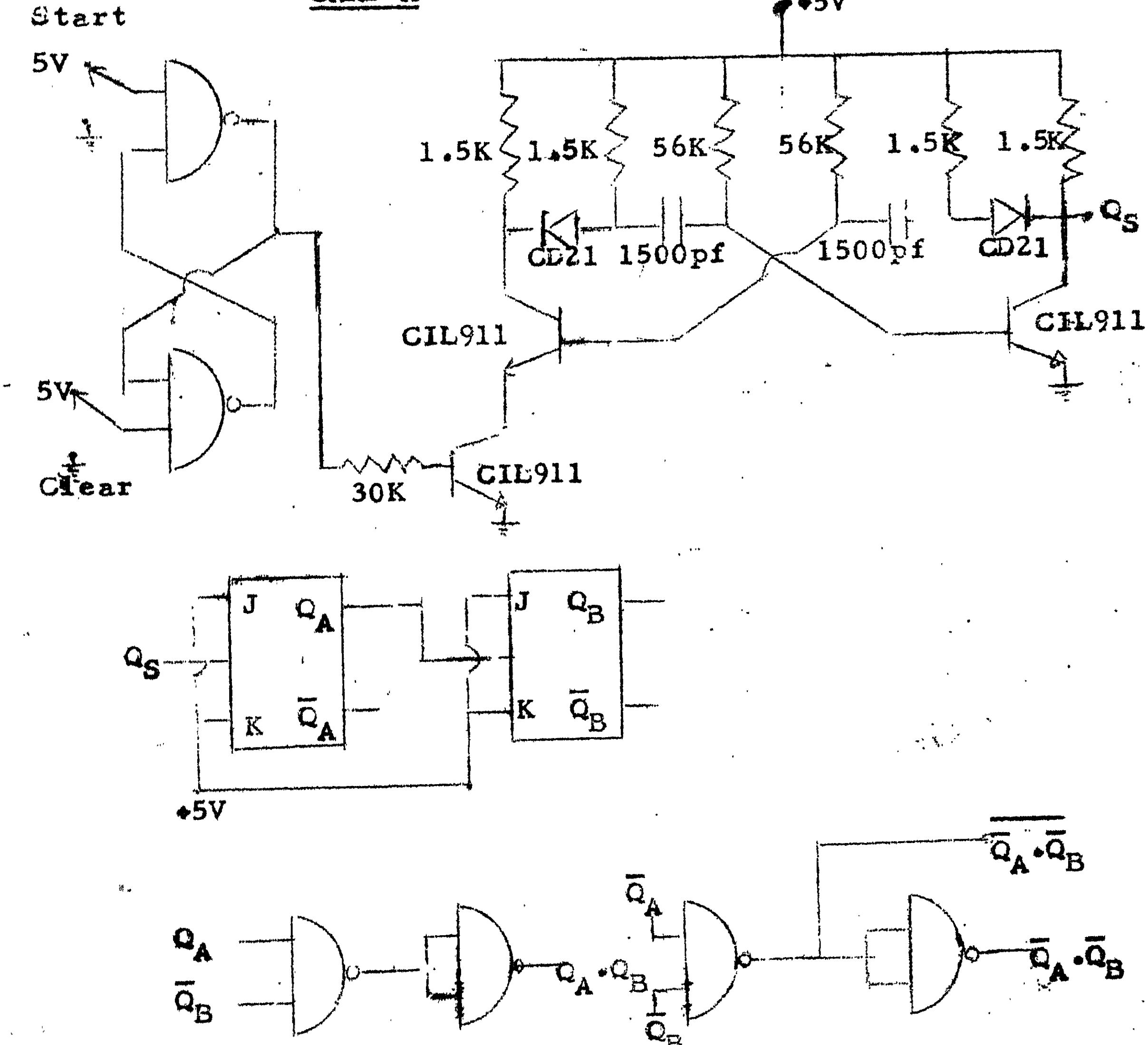



Fig. A-I.1.Gated **Astable**

## TABLE A-I.1

Pin Description CARD A

| Pin No | Description | Pin No | Description |
|---|---|---|---|
| 3 | $Q_B$ | 12 | $\bar{Q}_A \cdot \bar{Q}_B$ |
| 5 | $Q_A \cdot \bar{Q}_B$ | 14 | CLR |
| 7 | $\bar{Q}_B$ | 19 | Start |
| 10 | $\overline{\bar{Q}_A \cdot \bar{Q}_B}$ | | |

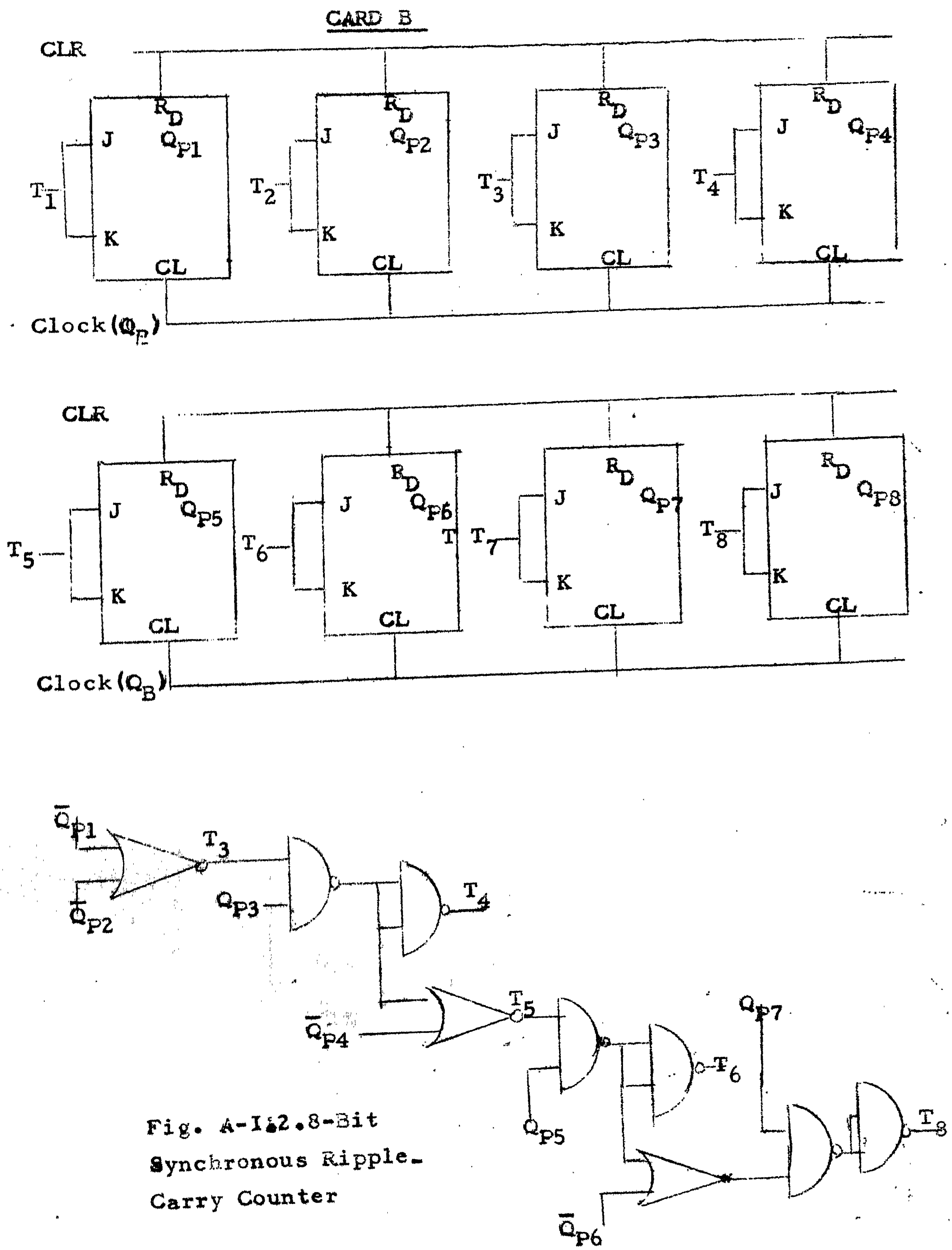



Fig. A-I.2.8-Bit Synchronous Ripple-Carry Counter

CARD B (Contd.)

LOGICAL EXPRESSIONS

| | | | | | |
|---|---|---|---|---|---|
| $T_1$ | = | 1 | $T_5$ | = | $Q_{P4} \cdot T_4$ |
| $T_2$ | = | $Q_{P1}$ | $T_6$ | = | $Q_{P5} \cdot T_5$ |
| $T_3$ | = | $Q_{P1} \cdot Q_{P2}$ | $T_7$ | = | $Q_{P6} \cdot T_6$ |
| $T_4$ | = | $Q_{P3} \cdot T_3$ | $T_8$ | = | $Q_{P7} \cdot T_7$ |

TABLE A-I.2

Pin Description, Card B

| Pin No. | Description | Pin No. | Description |
|---|---|---|---|
| 4 | $\bar{Q}_{P8}$ | 13 | $Q_{P4}$ |
| 5 | $Q_{P8}$ | 14 | $\bar{Q}_{P3}$ |
| 6 | $\bar{Q}_{P7}$ | 15 | $Q_{P3}$ |
| 7 | $Q_{P7}$ | 16 | $\bar{Q}_{P2}$ |
| 8 | $\bar{Q}_{P6}$ | 17 | $Q_{P2}$ |
| 9 | $Q_{P6}$ | 18 | $\bar{Q}_{P1}$ |
| 10 | $\bar{Q}_{P5}$ | 19 | $Q_{P1}$ |
| 11 | $Q_{P5}$ | 20 | $Q_B$ |
| 12 | $\bar{Q}_{P4}$ | 21 | CLR |

CARD C

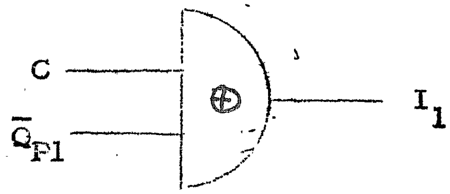
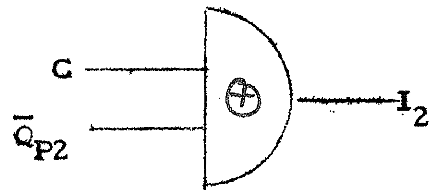



TABLE A-I.3

Pin Description Card C

| Pin No | Description |
|---|---|
| 2 | $Q_{P4}$ |
| 3 | $Q_{P3}$ |
| 4 | $\bar{Q}_{P2}$ |
| 5 | $\bar{Q}_{P1}$ |
| 6 | $I_1$ |
| 7 | $I_2$ |
| 8 | $I_3$ |
| 9 | $I_4$ |
| 18 | C |
| 19 | E |
| 20 | D |



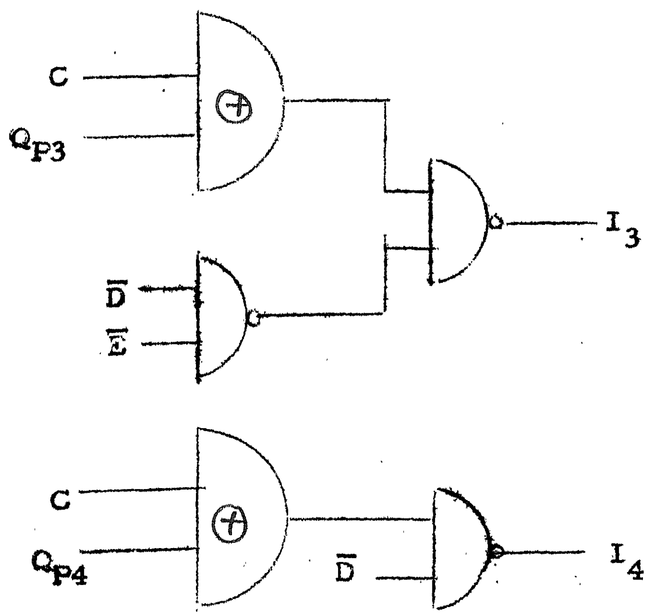




Fig.A-I.3.Reference Generator for Gates-I

CARD D

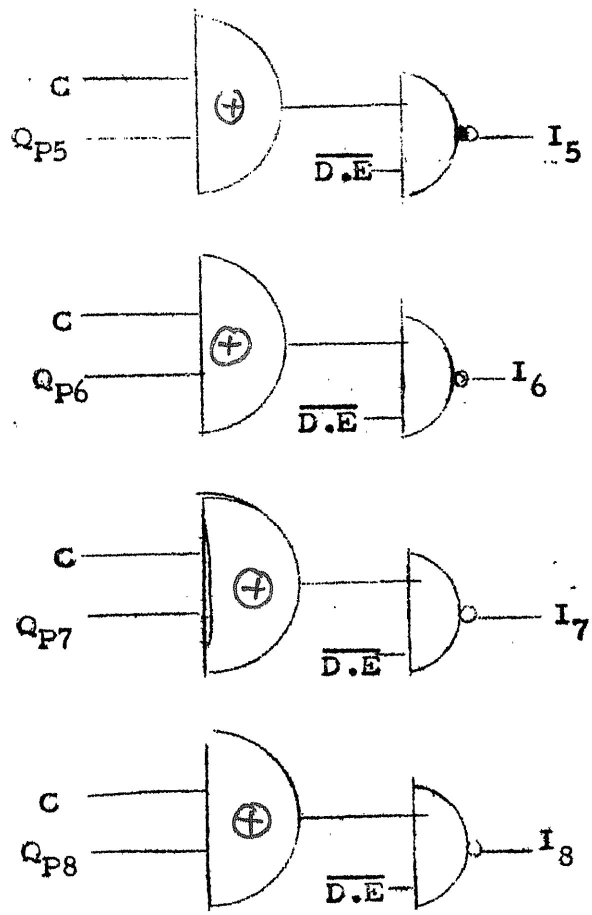



TABLE A-I.4

Pin Description Card D

| Pin No | Description | Pin No. | Description |
|---|---|---|---|
| 2 | $Q_{P7}$ | 12 | $I_7$ |
| 3 | $Q_{P8}$ | 13 | $I_8$ |
| 4 | $Q_{P6}$ | 18 | C |
| 5 | $Q_{P5}$ | 19 | D |
| 10 | $I_5$ | 20 | E |
| 11 | $I_6$ | | |

Fig. A-I.4.Reference Generator for Gates-II

CARD E

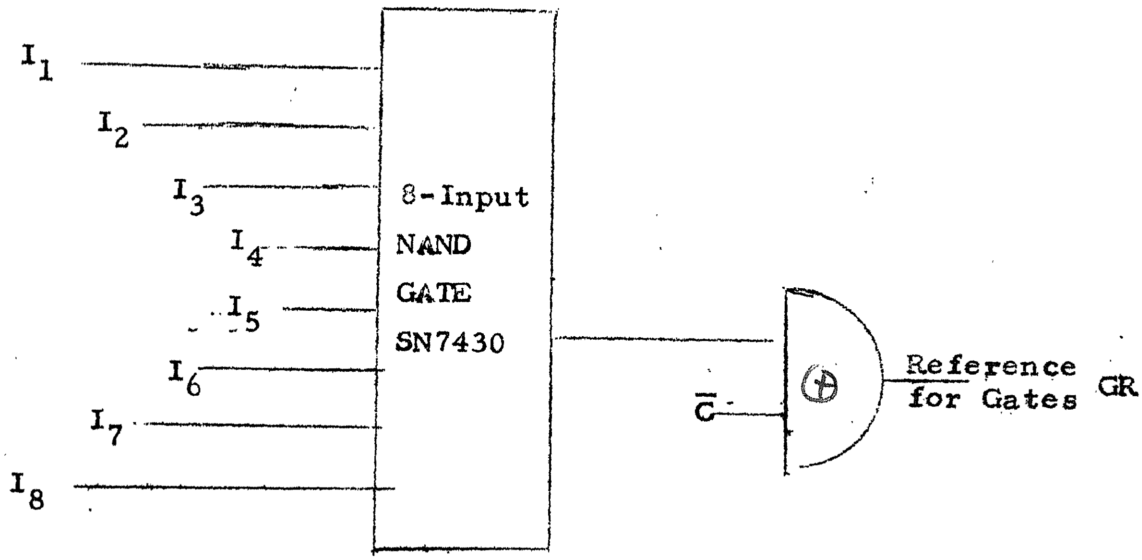


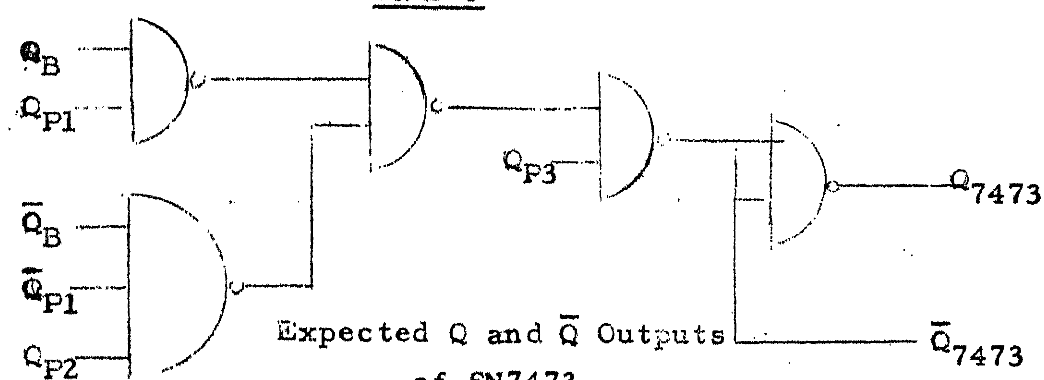

TABLE A-I.5

Pin Description Card E

| Pin No | Description | Pin No | Description |
|---|---|---|---|
| 2 | $I_1$ | 7 | $I_6$ |
| 3 | $I_2$ | 8 | $I_7$ |
| 4 | $I_3$ | 9 | $I_8$ |
| 5 | $I_4$ | 18 | $\bar{C}$ |
| 6 | $I_5$ | 21 | GR |

Fig. A-I.5.Reference Generator for Gates-III

## CARD F




Expected Q and $\bar{Q}$ Outputs of SN7473

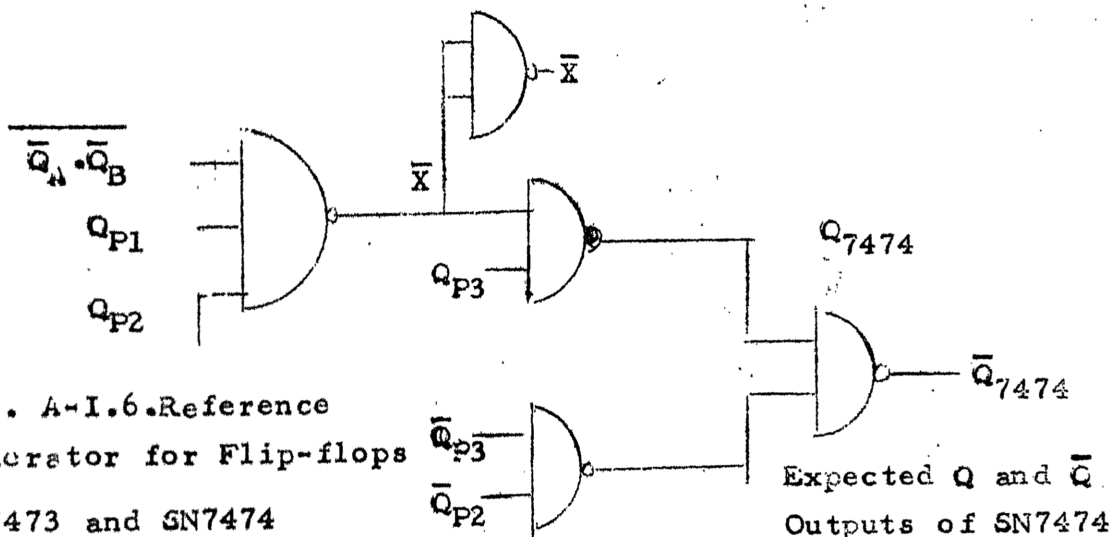



Fig. A-I.6. Reference Generator for Flip-flops SN7473 and SN7474

### TABLE A-I.6

| Pin No | Description | Pin No | Description |
|---|---|---|---|
| 5 | $\bar{Q}_A \cdot \bar{Q}_B$ | 13 | $\overline{\bar{Q}_A \cdot \bar{Q}_B}$ |
| 6 | $\bar{Y}$ | 14 | $\bar{Q}_{P3}$ |
| 7 | $\bar{Q}_{7474}$ | 15 | $Q_{P3}$ |
| 8 | $Q_{7474}$ | 16 | $\bar{Q}_{P2}$ |
| 9 | $Q_{7473}$ | 17 | $Q_{P2}$ |
| 10 | $\bar{Q}_{7473}$ | 18 | $\bar{Q}_{P1}$ |
| 11 | $\bar{X}$ | 19 | $Q_{P1}$ |
| 12 | X | 20 | $\bar{Q}_B$ |

CARD G

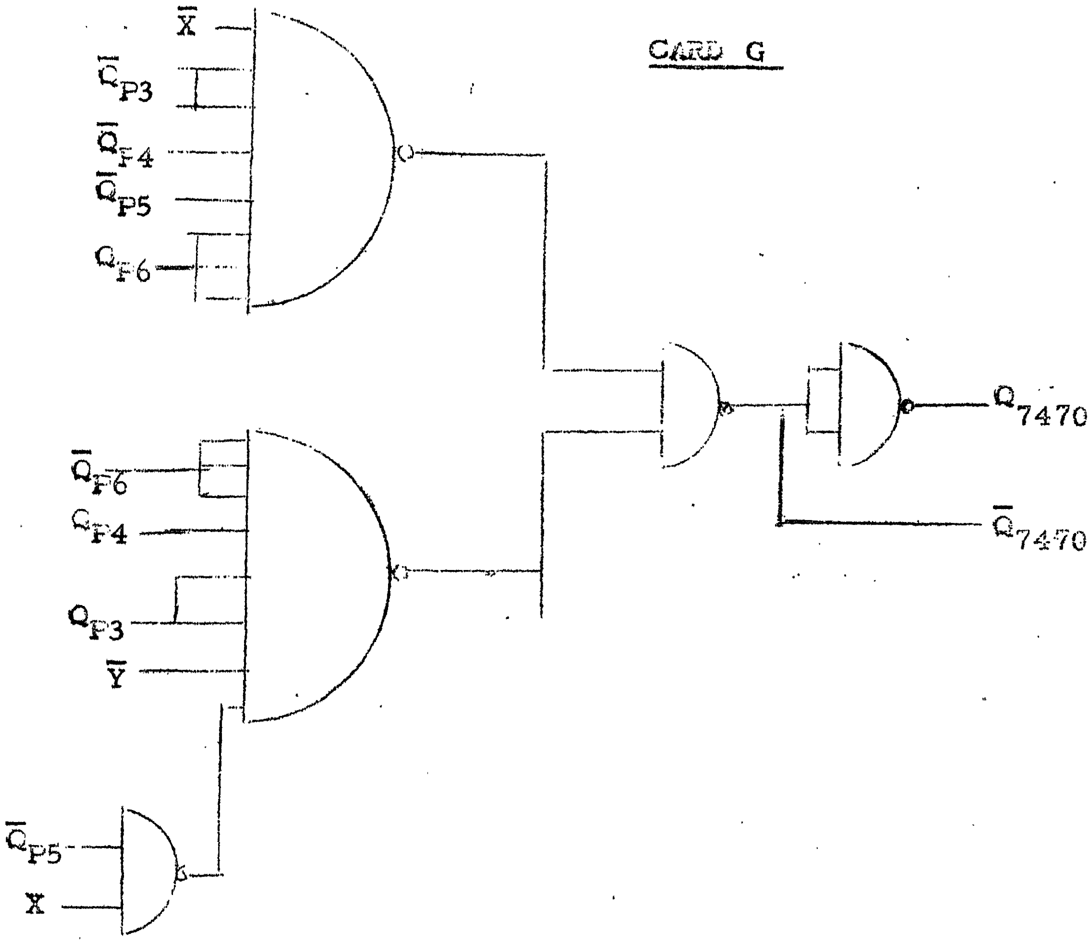


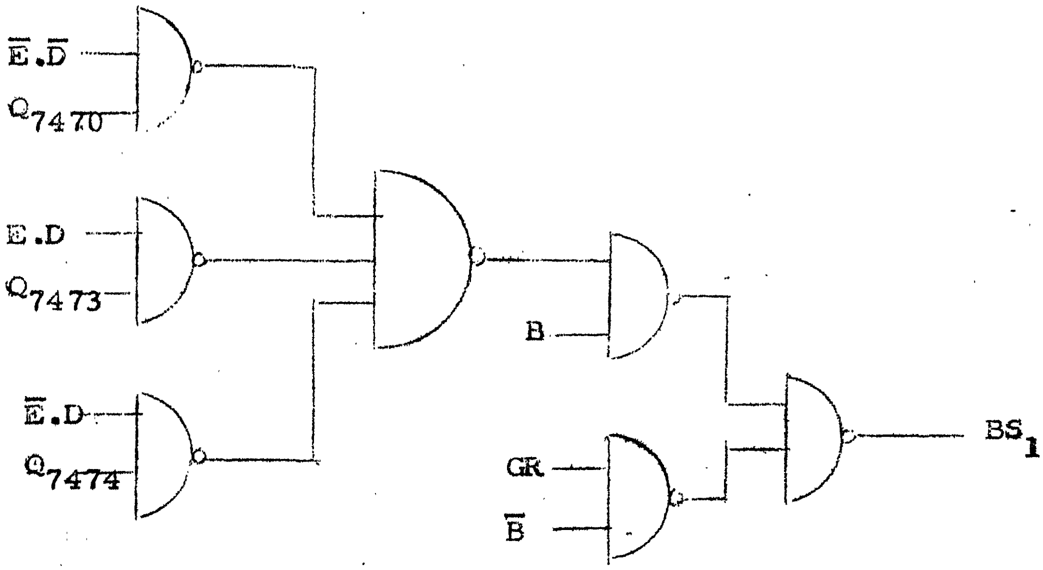

Fig.A-I.7.Reference Generator for SN7470

TABLE A-I.7

| Pin | Description | Pin | Description |
|---|---|---|---|
| 2 | $\overline{Q}_{P3}$ | 8 | $\overline{Q}_{P6}$ |
| 3 | $\overline{Q}_{P4}$ | 9 | $Q_{P3}$ |
| 4 | $\overline{Q}_{P5}$ | 10 | X |
| 5 | $Q_{P6}$ | 11 | Y |
| 6 | $\overline{X}$ | 16 | $Q_{7470}$ |
| 7 | $Q_{P4}$ | 17 | $\overline{Q}_{7470}$ |

## CARD H

$$BS_1 = B\,(\bar{D}.\bar{E}.Q_{7470} + D.E.\,Q_{7473} + D.\bar{E}.Q_{7474}) + \bar{B}.GR$$




$$BS_2 = B\,(\bar{D}.\bar{E}.\bar{Q}_{7470} + D.E.\bar{Q}_{7473} + D.\bar{E}.\bar{Q}_{7474}) + \bar{B}.GR$$

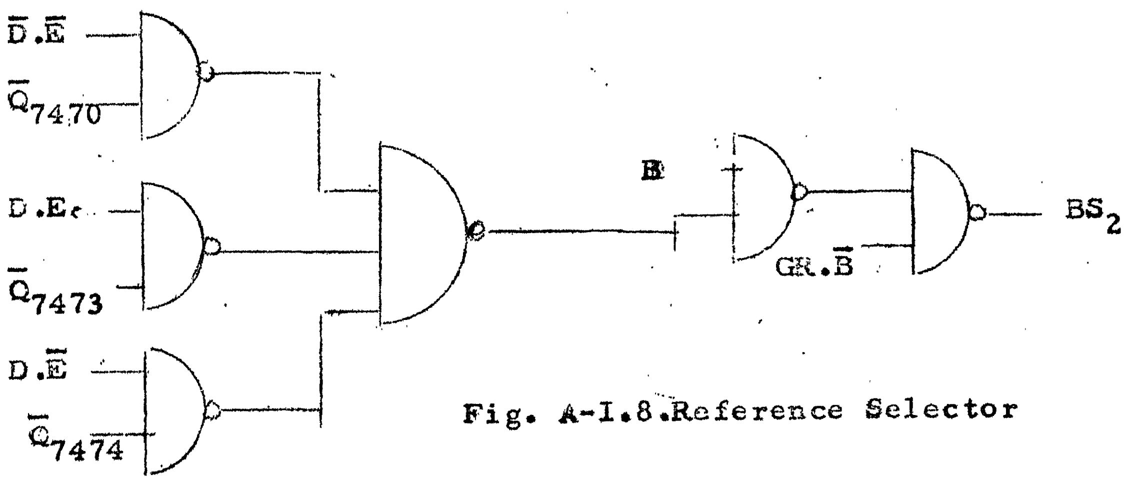



Fig. A-I.8.Reference Selector

CARD H (Contd.)

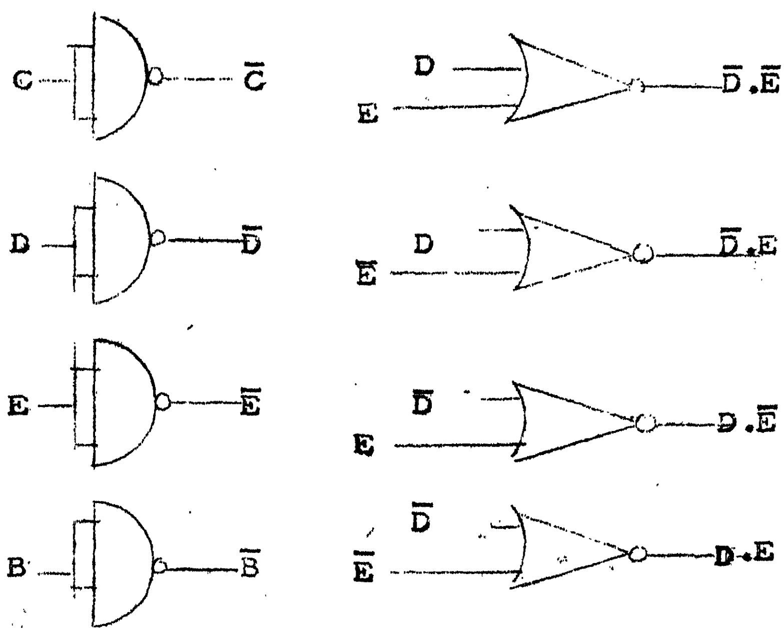



TABLE A-1.8

| Pin No | Description | Pin No | Description |
|---|---|---|---|
| 2 | C | 11 | $Q_{7473}$ |
| 3 | $\bar{C}$ | 12 | $Q_{7474}$ |
| 4 | D | 13 | $\bar{Q}_{7470}$ |
| 5 | $\bar{D}$ | 14 | $\bar{Q}_{7473}$ |
| 6 | B | 15 | $\bar{Q}_{7474}$ |
| 7 | $\bar{B}$ | 16 | GR |
| 9 | E | 17 | $BS_1$ |
| 10 | $Q_{7470}$ | 18 | $BS_2$ |

CARD J

TABLE A-I.9

| Pin No. | Description |
|---|---|
| 5 | CLR |
| 6 | $ER_4$ |
| 7 | $ER_3$ |
| 8 | $ER_2$ |
| 9 | $ER_1$ |
| 10 | $\overline{B}$ |
| 11 | E |
| 12 | $\overline{D}$ |
| 13 | D |
| 14 | $O_4$ |
| 15 | $R_4$ |
| 16 | $O_3$ |
| 17 | $R_3$ |
| 18 | $O_2$ |
| 19 | $R_2$ |
| 20 | $O_1$ |
| 21 | $R_1$ |

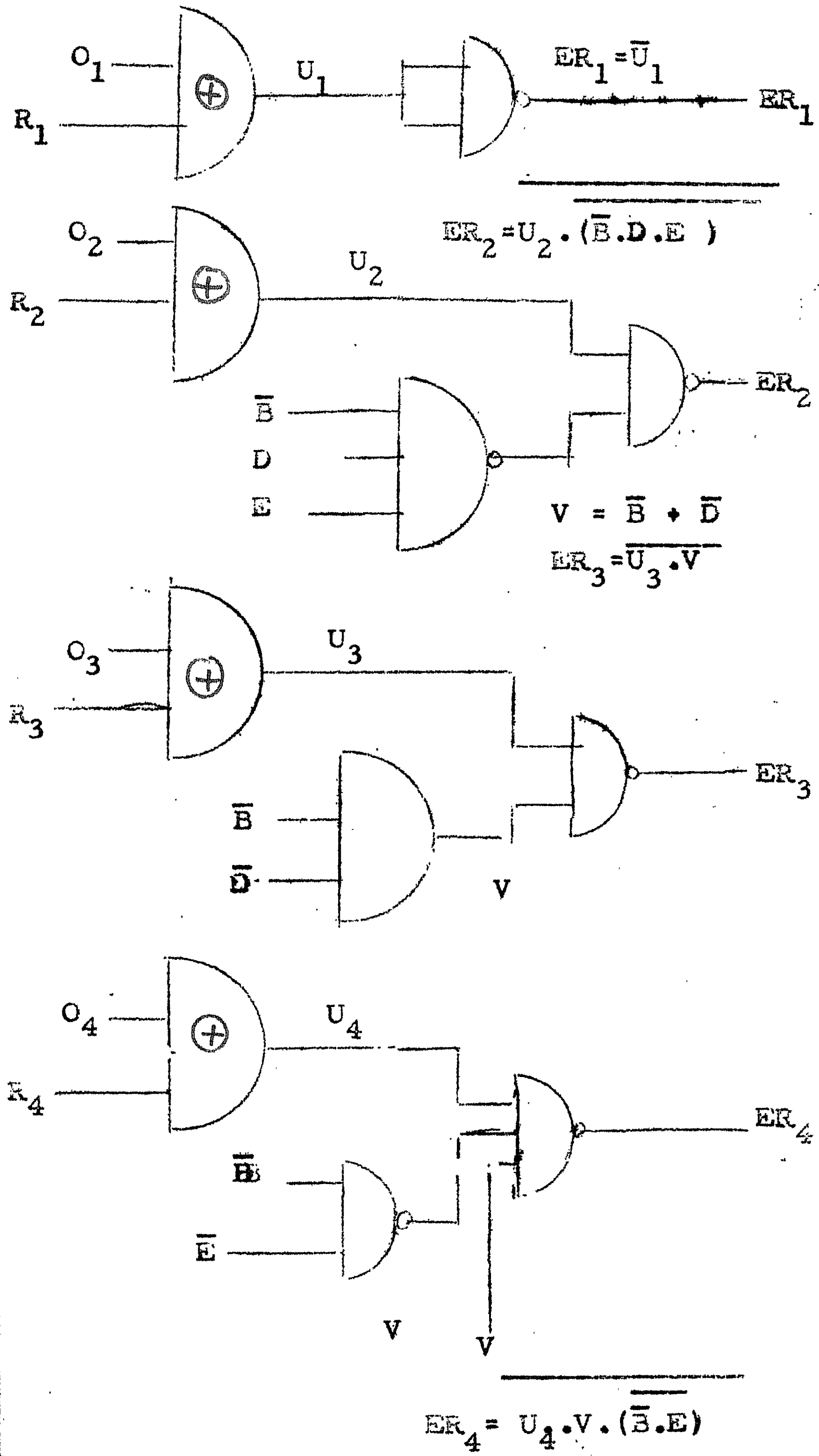



Fig.A-I.9.Comparators and Error Latches

CARD K

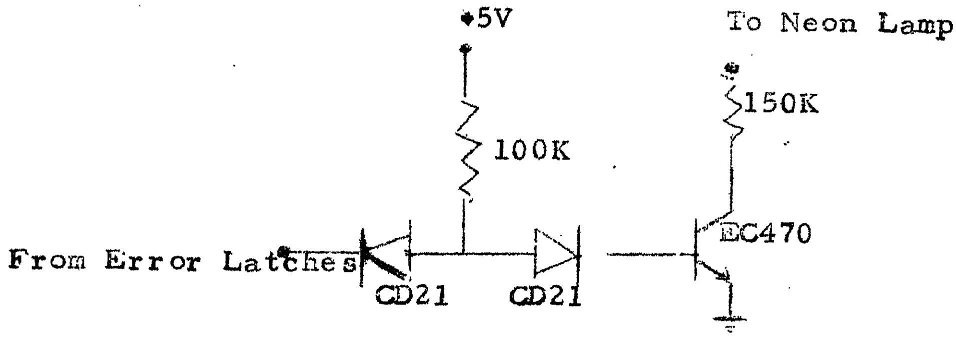



Fig.A-I.10.Reject Lamp Driver

TABLE A-I.10

| Pin No. | Descrip-tion | Pin No. | Descrip-tion |
|---|---|---|---|
| 2 | $ER_1$ | 8 | $ER_3$ |
| 3 | $L_1$ | 10 | $L_3$ |
| 5 | $ER_2$ | 13 | $ER_4$ |
| 6 | $L_2$ | 15 | $L_4$ |

## APPENDIX-II

The various interconnections of the twenty two pins of each card are given in Table A-II.1. The letter A,B,C,D,E,F,G,H,J,K,L followed by a number represents the card and the pin number on that card respectively. For example D5 represents card D and pin 5. The connections diagram for the Band Switch, used for selecting either internal or external reference is shown in Fig.A-II.1.

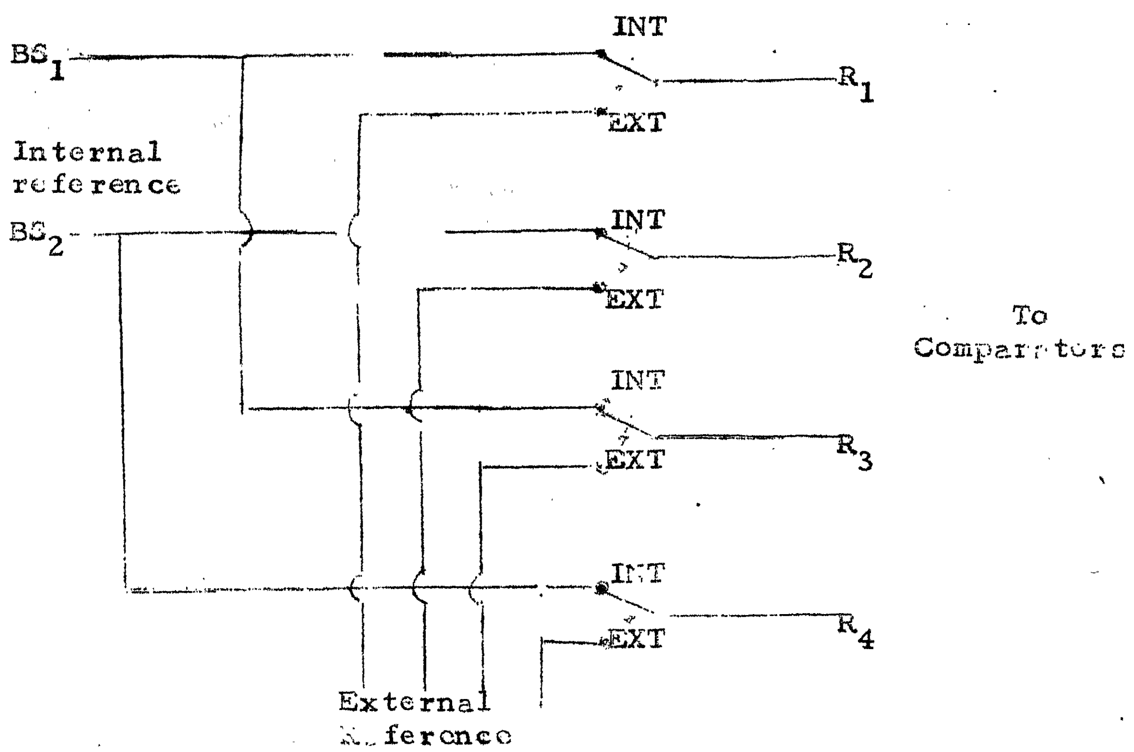



Fig. A-II.1.Band Switch Connection Diagram

TABLE A-II.1

| PIN | CARD A | CARD B | CARD C | CARD D |
|---|---|---|---|---|
| 1 | GND | GND | GND | GND |
| 2 | | | B13 | B7 |
| 3 | B20 | - | B15 | B5 |
| 4 | - | - | B16 | B9 |
| 5 | CC14 | $P_8$,$D_3$ | B18 | B11 |
| 6 | - | - | E2 | - |
| 7 | F20 | $P_7$,$D_2$ | E3 | - |
| 8 | - | G8 | E4 | - |
| 9 | - | $P_6$,$D_4$ | E5 | - |
| 10 | F13 | G4 | - | E6 |
| 11 | - | $P_5$,D5 | - | E7 |
| 12 | F5 | G3 | - | E8 |
| 13 | - | $P_4$,C2 | - | E9 |
| 14 | CLR, B21 | F14 | - | - |
| 15 | - | $P_3$,C3 | - | - |
| 16 | - | C4 | - | - |
| 17 | - | $P_2$,F17 | - | - |
| 18 | - | $C_5$ | CC18,D18 | C18 |
| 19 | ST | $P_1$, F19 | CC20,D20 | C20 |
| 20 | - | F21 | CC19,D19 | C19 |
| 21 | - | J5 | - | - |
| 22 | VCC | VCC | VCC | VCC |

TABLE A-II.1 (Contd.)

| PIN | CARD E | CARD F | CARD G | CARD H |
|---|---|---|---|---|
| 1 | GND | GND | GND | GND |
| 2 | G6 | - | F14 | D18 |
| 3 | C7 | - | B12 | E18 |
| 4 | C8 | - | B10 | D19 |
| 5 | C9 | A12 | B9 | J12 |
| 6 | D10 | F11 | F11 | CC17 |
| 7 | D11 | A15 | B13 | J10 |
| 8 | D12 | H12 | B8 | D20 |
| 9 | D13 | H11 | F15 | - |
| 10 | - | H14 | F12 | G16 |
| 11 | - | G6 | F6 | F9 |
| 12 | - | G10 | - | F8 |
| 13 | - | A10 | - | G17 |
| 14 | - | B14 | - | F10 |
| 15 | - | B15 | - | F7 |
| 16 | - | B16 | H10 | E21 |
| 17 | - | B17 | H13 | $BS_1$ |
| 18 | H3 | B18 | - | $BS_2$ |
| 19 | - | B19 | - | - |
| 20 | - | A7 | | |
| 21 | - | B20 | - | - |
| 22 | VCC | VCC | VCC | VCC |

TABLE A.II.1 (Contd.)

| PIN | CARD J | CARD K | CARD L |
|---|---|---|---|
| 1 | GND | GND | GND |
| 2 | - | J9 | - |
| 3 | - | $L_1$ | - |
| 4 | - | - | - |
| 5 | B21 | J8 | - |
| 6 | K13 | $L_2$ | - |
| 7 | K8 | - | - |
| 8 | K5 | J7 | - |
| 9 | K2 | - | - |
| 10 | H7 | $L_3$ | - |
| 11 | H8 | - | - |
| 12 | H5 | - | - |
| 13 | H4 | J6 | - |
| 14 | CC13 ,$O_4$ | - | - |
| 15 | BS,$R_4$ | $L_4$ | - |
| 16 | CC12,$O_3$ | - | - |
| 17 | BS,$R_3$ | - | - |
| 18 | CC11,$O_2$ | - | - |
| 19 | BS,$R_2$ | - | - |
| 20 | CC10,$0_1$ | - | - |
| 21 | BS,$R_1$ | - | - |
| 22 | VCC | VCC | VCC |

## APPENDIX-III

## OPERATING INSTRUCTIONS

A procedure for using the tester is given below

1) Switch-on the mains.

2) Press Clear (CLR) button. This should clear all the reject lamps.

3) If the circuit card is available for the IC, then

a) put the Band-switch (B.S.) to INT position.

b) Insert the correct circuit card into the 22 pin connector on the panel.

c) Push the IC into the IC base on the circuit card.

Otherwise,

a) Put the B.S. to EXT position.

b) Patch up as desired using the patch board card available.

c) Insert this card into the 22 pin connector on the panel.

d) Push the IC into the IC base on this card

4) Press start button.

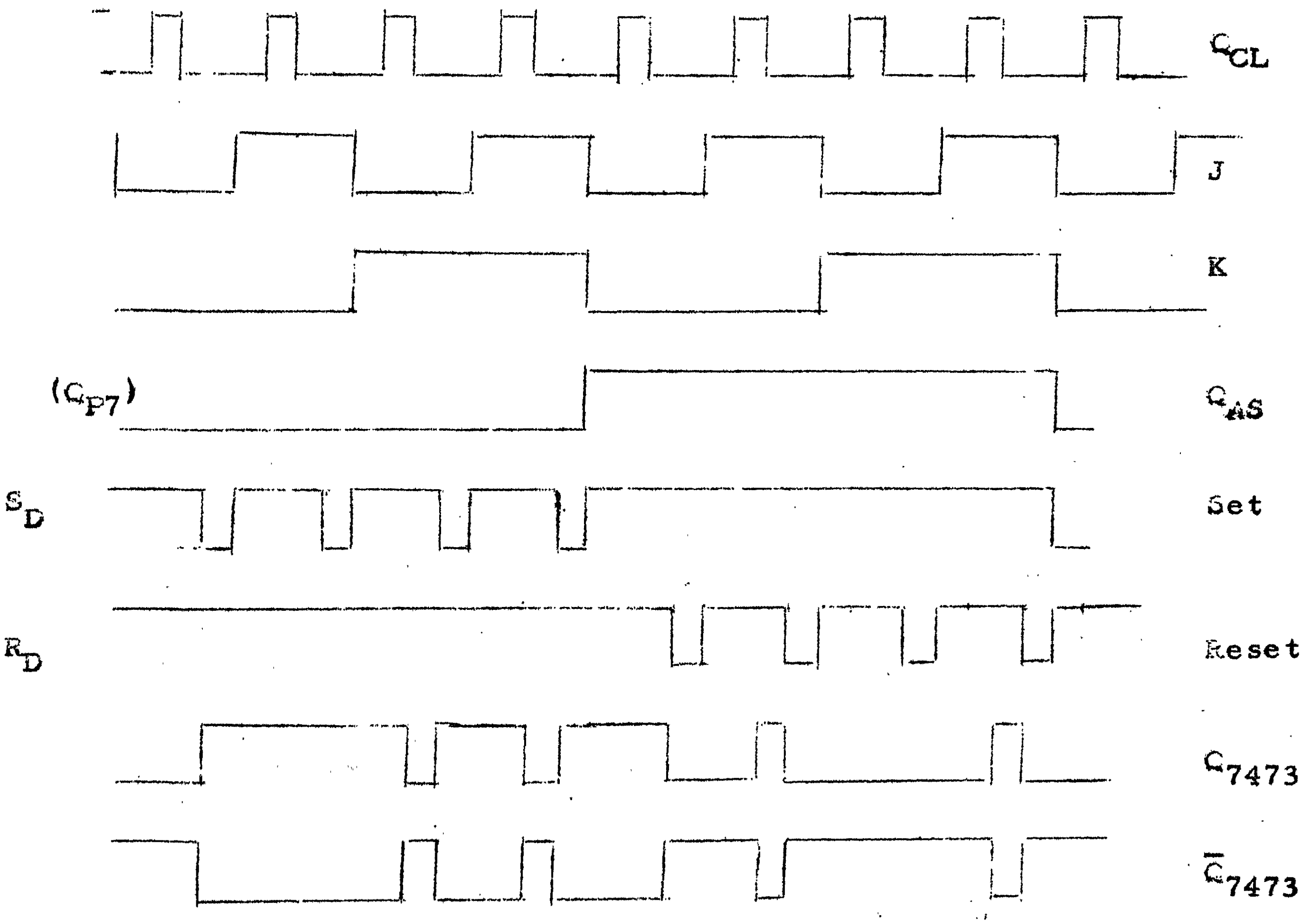
5) If no reject lamp is ON the IC is functionally good. If any reject lamp/lamps is/are ON, then

a) In the case of gates, the lamp numbers indicate the corresponding malfunctioning gates.

b) In the case of flip-flops, the lamps 1 and 2 indicate the conditions of Q and $\overline{Q}$ of flip-flop 1 and lamps 3 and 4 correspond to Q & $\overline{Q}$ of FF 2, if any.

## APPENDIX - IV

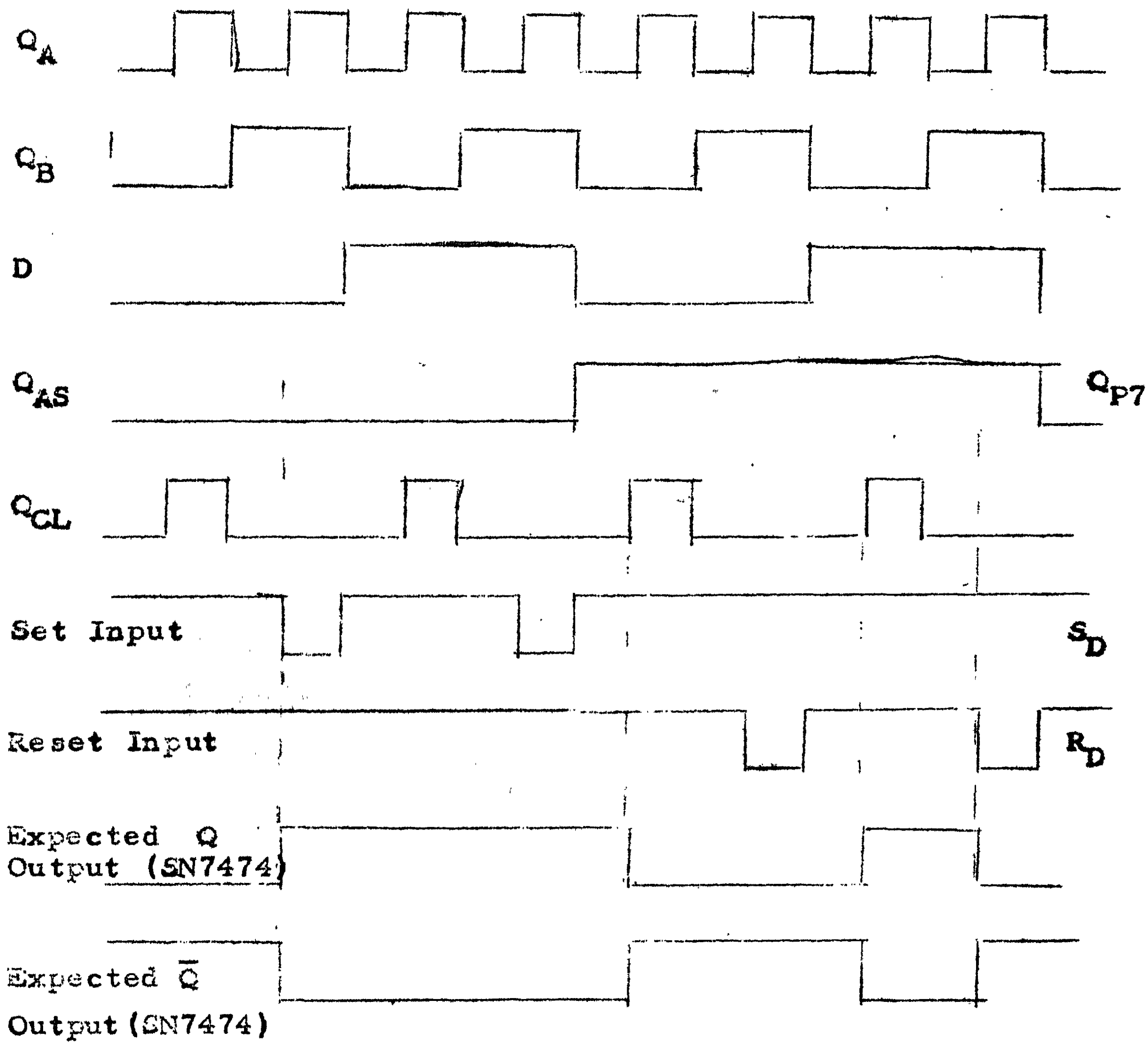
An alternate scheme of testing flip-flops in which the initial state of the flip-flop is brought to either 1 or 0 (by appling appropriate Set or Reset pulses) before the application of every clock pulse is given here. Set input of the flip-flop is obtained as $(\overline{Q_A \cdot Q_B})\ \overline{Q_{P7}}$ while Reset input is obtained as $(\overline{Q_A \cdot Q_B}) \cdot Q_{P7}$ so that Set input is tested during $\overline{Q_{P7}}$ while Reset input is tested during $Q_{P7}$. This also takes care that edge of any asynchronous input does not interfere in the enabling edge of the clock. The waveforms and the logical expressions for the expected outputs for two types of flip-flops (SN7473 and SN7474) are shown in Fig. A-IV.1. Set and Reset inputs of the flip-flop are to be brought to pins 8 and 9 of the 22 pin connector. This requires the modification of the actual input 7 applied to D.U.T. as $\overline{B} \cdot Q_{P7} + B \cdot Q_{P7} \cdot (\overline{Q_A \cdot Q_B})$ and input 8 as $\overline{B} \cdot Q_{P8} + B \cdot Q_{P7} (\overline{Q_A \cdot Q_B})$.




$$Q_{7473} = \bar{Q}_{AS}\,(\bar{S}_D + \bar{Q}_B \cdot K + J \cdot \bar{K}) + Q_{AS}\,(\bar{Q}_A \cdot Q_B) \cdot J + \bar{J} \cdot \bar{K}\,(\overline{Q_A \cdot Q_B})$$

$$\bar{Q}_{7473} = \overline{Q_{7473}}$$

Fig. A-IV.1(a). Flip-flop Testing; Alternate Scheme (SN7473)




$$Q_{7474} = \overline{Q}_{AS}(D+\overline{S}_D) + Q_{AS}(\overline{D}\cdot\overline{\overline{Q}_A\cdot\overline{Q}_B}+ D(Q_A+Q_B))$$

$$\overline{Q}_{7474} = \overline{Q_{7474}}$$

Fig. A-IV.1(b) Flip-flop Testing; Alternate Scheme (SN 7474)

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2. Electronics Design. Special issue onIC Testing., September 1968.

3. Frederick Van Veen., 'An introduction to IC Testing', IEEE Spectrum, pp 28-37,December 1971.

4. R.L.Morris and J.R.Miller., 'Designing with TTL Integrated Circuits', McGraw Hill Book Company.